

Annex K: Serial Presence Detect (SPD) for DDR3 SDRAM Modules

DDR3 SPD

Document Release 6

UDIMM Revision 1.3

RDIMM Revision 1.3

CDIMM Revision 1.3

LRDIMM Revision 1.2

1.0 Introduction

This annex describes the serial presence detect (SPD) values for all DDR3 modules. Differences between module types are encapsulated in subsections of this annex. These presence detect values are those referenced in the SPD standard document for 'Specific Features'. The following SPD fields will be documented in the order presented in section 1.1 with the exception of bytes 60 ~ 116 which are documented in separate appendices, one for each family of module types. Further description of Byte 2 is found in annex A of the SPD standard. All unused entries will be coded as 0x00. All unused bits in defined bytes will be coded as 0 except where noted.

To allow for maximum flexibility as devices evolve, SPD fields described in this document may support device configuration and timing options that are not included in the JEDEC DDR3 SDRAM data sheet (JESD79-3). Please refer to DRAM supplier data sheets or JESD79-3 to determine the compatibility of components.

1.1 Address map

The following is the SPD address map for all DDR3 modules. It describes where the individual lookup table entries will be held in the serial EEPROM.

| Byte Number | Function Described | Notes |
|-------------|--|-------|
| 0 | Number of Serial PD Bytes Written / SPD Device Size / CRC Coverage | 1, 2 |
| 1 | SPD Revision | |
| 2 | Key Byte / DRAM Device Type | |
| 3 | Key Byte / Module Type | |
| 4 | SDRAM Density and Banks | 3 |
| 5 | SDRAM Addressing | 3 |
| 6 | Module Nominal Voltage, VDD | |
| 7 | Module Organization | 3 |
| 8 | Module Memory Bus Width | |
| 9 | Fine Timebase (FTB) Dividend / Divisor | |
| 10 | Medium Timebase (MTB) Dividend | |
| 11 | Medium Timebase (MTB) Divisor | |
| 12 | SDRAM Minimum Cycle Time (tCKmin) | 3 |
| 13 | Reserved | |
| 14 | CAS Latencies Supported, Least Significant Byte | 3 |
| 15 | CAS Latencies Supported, Most Significant Byte | 3 |

Note 1 Number of SPD bytes written will typically be programmed as 128 or 176 bytes.
Note 2 Size of SPD device will typically be programmed as 256 bytes.
Note 3 From DDR3 SDRAM datasheet.
Note 4 These are optional, in accordance with the JEDEC spec.

| Byte Number | Function Described | Notes |
|---|--|-------|
| 16 | Minimum CAS Latency Time (tAAmin) | 3 |
| 17 | Minimum Write Recovery Time (tWRmin) | 3 |
| 18 | Minimum RAS# to CAS# Delay Time (tRCDmin) | 3 |
| 19 | Minimum Row Active to Row Active Delay Time (tRRDmin) | 3 |
| 20 | Minimum Row Precharge Delay Time (tRPmin) | 3 |
| 21 | Upper Nibbles for tRAS and tRC | 3 |
| 22 | Minimum Active to Precharge Delay Time (tRASmin), Least Significant Byte | 3 |
| 23 | Minimum Active to Active/Refresh Delay Time (tRCmin), Least Significant Byte | 3 |
| 24 | Minimum Refresh Recovery Delay Time (tRFCmin), Least Significant Byte | 3 |
| 25 | Minimum Refresh Recovery Delay Time (tRFCmin), Most Significant Byte | 3 |
| 26 | Minimum Internal Write to Read Command Delay Time (tWTRmin) | 3 |
| 27 | Minimum Internal Read to Precharge Command Delay Time (tRTPmin) | 3 |
| 28 | Upper Nibble for tFAW | 3 |
| 29 | Minimum Four Activate Window Delay Time (tFAWmin) | 3 |
| 30 | SDRAM Optional Features | 3 |
| 31 | SDRAM Thermal and Refresh Options | 3 |
| 32 | Module Thermal Sensor | |
| 33 | SDRAM Device Type | |
| 34 | Fine Offset for SDRAM Minimum Cycle Time (tCKmin) | |
| 35 | Fine Offset for Minimum CAS Latency Time (tAAmin) | |
| 36 | Fine Offset for Minimum RAS# to CAS# Delay Time (tRCDmin) | |
| 37 | Fine Offset for Minimum Row Precharge Delay Time (tRPmin) | |
| 38 | Fine Offset for Minimum Active to Active/Refresh Delay Time (tRCmin) | |
| 39 ~ 40 | Reserved, General Section | |
| 41 | SDRAM Maximum Activate Count (MAC) Value | 3 |
| 42 ~ 59 | Reserved, General Section | |
| 60 ~ 116 | Module Type Specific Section, Indexed by Key Byte 3 | |
| 117 ~ 118 | Module ID: Module Manufacturer's JEDEC ID Code | |
| 119 | Module ID: Module Manufacturing Location | |
| 120 ~ 121 | Module ID: Module Manufacturing Date | |
| 122 ~ 125 | Module ID: Module Serial Number | |
| 126 ~ 127 | Cyclical Redundancy Code | |
| 128 ~ 145 | Module Part Number | 4 |
| 146 ~ 147 | Module Revision Code | 4 |
| 148 ~ 149 | DRAM Manufacturer's JEDEC ID Code | 4 |
| 150 ~ 175 | Manufacturer's Specific Data | 4 |
| 176 ~ 255 | Open for customer use | |
| <p>Note 1 Number of SPD bytes written will typically be programmed as 128 or 176 bytes. Note 2 Size of SPD device will typically be programmed as 256 bytes. Note 3 From DDR3 SDRAM datasheet. Note 4 These are optional, in accordance with the JEDEC spec.</p> | | |

2.0 Details of each byte

2.1 General Section: Bytes 0 to 59

This section contains defines bytes that are common to all DDR3 module types.

Byte 0: Number of Bytes Used / Number of Bytes in SPD Device / CRC Coverage

The least significant nibble of this byte describes the total number of bytes used by the module manufacturer for the SPD data and any (optional) specific supplier information. The byte count includes the fields for all required and optional data. Bits 6 ~ 4 describe the total size of the serial memory used to hold the Serial Presence Detect data. Bit 7 indicates whether the unique module identifier (found in bytes 117 ~ 125) is covered by the CRC encoded on bytes 126 and 127.

| Bit 7 | Bits 6 ~ 4 | Bits 3 ~ 0 |
|--|--|---|
| CRC Coverage | SPD Bytes Total | SPD Bytes Used |
| 0 = CRC covers bytes 0 ~ 125 1 = CRC covers bytes 0 ~ 116 | Bit [6, 5, 4] : 000 = Undefined 001 = 256 All others reserved | Bit [3, 2, 1, 0] : 0000 = Undefined 0001 = 128 0010 = 176 0011 = 256 All others reserved |

Byte 1: SPD Revision

This byte describes the compatibility level of the encoding of the bytes contained in the SPD EEPROM, and the current collection of valid defined bytes. Software should examine the upper nibble (Encoding Level) to determine if it can correctly interpret the contents of the module SPD. The lower nibble (Additions Level) can optionally be used to determine which additional bytes or attribute bits have been defined; however, since any undefined additional byte must be encoded as 0x00 or undefined attribute bit must be defined as 0, software can safely detect additional bytes and use safe defaults if a zero encoding is read for these bytes.

| Production Status | SPD Revision | Encoding Level | | | | Additions Level | | | | Hex |
|-------------------|--------------|----------------|-------|-------|-------|-----------------|-------|-------|-------|-----|
| | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | |
| Pre-production | Revision 0.0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 |
| | Revision 0.1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01 |
| | ... | . | . | . | . | . | . | . | . | . |
| | Revision 0.9 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 09 |
| Production | Revision 1.0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10 |
| | Revision 1.1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 11 |
| | ... | . | . | . | . | . | . | . | . | ... |
| Undefined | Undefined | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | FF |

The Additions Level is never reduced even after an increment of the Encoding Level. For example, if the current SPD revision level were 1.2 and a change in Encoding Level were approved, the next revision level would be 2.2. If additions to revision 2.2 were approved, the next revision would be 2.3. Changes in the Encoding Level are extremely rare, however, since they can create incompatibilities with older systems.

The exceptions to the above rule are the SPD revision levels used during development prior to the Revision 1.0 release. Revisions 0.0 through 0.9 are used to indicate sequential pre-production SPD revision levels, however the first production release will be Revision 1.0.

Release 24

This document defines the SPD contents for multiple families of DDR3 memory modules, with a separate subsection for each family that defines the bytes in SPD locations 60~116. These module families and their respective subsections are:

- Annex K.1: Unbuffered Memory Modules
- Annex K.2: Registered Memory Modules
- Annex K.3: Clocked Memory Modules
- Annex K.4: Load Reduced Memory Modules

The SPD revision level for each module family type is independent. This allows changes to be made to the Registered DIMM annex, for example, without necessarily changing the revision of Unbuffered DIMMs. In this context, the SPD revision value corresponds to all SPD bytes *for that DIMM type*. It also means that over time, the revisions for each module type may vary. Note that changes to a DIMM specific annex does not affect the revisions of other module types, but changes in the General Section of the SPD affect all DIMM types. The following example suggests a possible historical progression:

TABLE 1. Hypothetical Historic Progression of SPD Revisions by DIMM Type

| Event | UDIMM | RDIMM | CDIMM | LRDIMM |
|------------------------------------|-------|-------|-------|--------|
| Initial SPD release | 1.0 | 1.0 | 1.0 | 1.0 |
| Addition in RDIMM Annex | 1.0 | 1.1 | 1.0 | 1.0 |
| Addition in LRDIMM Annex | 1.0 | 1.1 | 1.0 | 1.1 |
| Addition in LRDIMM Annex | 1.0 | 1.1 | 1.0 | 1.2 |
| Addition in General Section | 1.1 | 1.2 | 1.1 | 1.3 |
| Addition in UDIMM Annex | 1.2 | 1.2 | 1.1 | 1.3 |
| Encoding change in LRDIMM Annex | 1.2 | 1.2 | 1.1 | 2.3 |
| Addition in LRDIMM Annex | 1.2 | 1.2 | 1.1 | 2.4 |
| Encoding change in General Section | 2.2 | 2.2 | 2.1 | 3.4 |
| Addition in RDIMM Annex | 2.2 | 2.3 | 2.1 | 3.4 |

Byte 2: Key Byte / DRAM Device Type

This byte is the key byte used by the system BIOS to determine how to interpret all other bytes in the SPD EEPROM. The BIOS must check this byte first to ensure that the EEPROM data is interpreted correctly. Any DRAM or Module type that requires significant changes to the SPD format (beyond defining previously undefined bytes or bits) also requires a new entry in the key byte table below.

| Line # | SDRAM / Module Type Corresponding to Key Byte | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Hex |
|--------|---|-------|-------|-------|-------|-------|-------|-------|-------|-----|
| 0 | Reserved | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 |
| 1 | Standard FPM DRAM | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01 |
| 2 | EDO | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 02 |
| 3 | Pipelined Nibble | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 03 |
| 4 | SDRAM | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 04 |
| 5 | ROM | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 05 |
| 6 | DDR SGRAM | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 06 |
| 7 | DDR SDRAM | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 07 |
| 8 | DDR2 SDRAM | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 08 |
| 9 | DDR2 SDRAM FB-DIMM | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 09 |

| Line # | SDRAM / Module Type Corresponding to Key Byte | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Hex |
|--------|---|-------|-------|-------|-------|-------|-------|-------|-------|-----|
| 10 | DDR2 SDRAM FB-DIMM PROBE | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0A |
| 11 | DDR3 SDRAM | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0B |
| - | - | - | - | - | - | - | - | - | - | - |
| 253 | Reserved | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | FD |
| 254 | Reserved | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | FE |
| 255 | Reserved | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | FF |

Byte 3: Key Byte / Module Type

This byte is a Key Byte used to index the module specific section of the SPD from bytes 60 ~ 116. Byte 3 identifies the SDRAM memory module type which implies the width (D dimension) of the module. Other module physical characteristics, such as height (A dimension) or thickness (E dimension) are documented in the module specific section of the SPD. Refer to the relevant JEDEC JC-11 module outline (MO) documents for dimension definitions.

| Bits 7 ~ 4 | Bits 3 ~ 0 |
|---|--|
| Reserved | Module Type |
| | Bit [3, 2, 1, 0] : 0000 = Undefined 0001 = RDIMM (width = 133.35 mm nom) 0010 = UDIMM (width = 133.35 mm nom) 0011 = SO-DIMM (width = 67.6 mm nom) 0100 = Micro-DIMM (width = TBD mm nom) 0101 = Mini-RDIMM (width = 82.0 mm nom) 0110 = Mini-UDIMM (width = 82.0 mm nom) 0111 = Mini-CDIMM (width = 67.6 mm nom) 1000 = 72b-SO-UDIMM (width = 67.6 mm nom) 1001 = 72b-SO-RDIMM (width = 67.6 mm nom) 1010 = 72b-SO-CDIMM (width = 67.6 mm nom) 1011 = LRDIMM (width = 133.35 mm nom) 1100 = 16b-SO-DIMM (width = 67.6 mm nom) 1101 = 32b-SO-DIMM (width = 67.6 mm nom) All others reserved |
| Definitions: RDIMM: Registered Dual In-Line Memory Module LRDIMM: Load Reduced Dual In-Line Memory Module UDIMM: Unbuffered Dual In-Line Memory Module SO-DIMM: Unbuffered 64-bit Small Outline Dual In-Line Memory Module Micro-DIMM: Micro Dual In-Line Memory Module Mini-RDIMM: Mini Registered Dual In-Line Memory Module Mini-UDIMM: Mini Unbuffered Dual In-Line Memory Module Mini-CDIMM: Clocked 72-bit Mini Dual In-Line Memory Module 72b-SO-UDIMM: Unbuffered 72-bit Small Outline Dual In-Line Memory Module 72b-SO-RDIMM: Registered 72-bit Small Outline Dual In-Line Memory Module 72b-SO-CDIMM: Clocked 72-bit Small Outline Dual In-Line Memory Module 16b-SO-DIMM: Unbuffered 16-bit Small Outline Dual In-Line Memory Module 32b-SO-DIMM: Unbuffered 32-bit Small Outline Dual In-Line Memory Module | |

Byte 4: SDRAM Density and Banks

This byte defines the total density of the DDR3 SDRAM, in bits, and the number of internal banks into which the memory array is divided. These values come from the DDR3 SDRAM data sheet.

| Bit 7 | Bits 6 ~ 4 | Bits 3 ~ 0 |
|----------|---|---|
| Reserved | Bank Address Bits | Total SDRAM capacity, in megabits |
| | Bit [6, 5, 4] : 000 = 3 (8 banks) 001 = 4 (16 banks) 010 = 5 (32 banks) 011 = 6 (64 banks) All others reserved | Bit [3, 2, 1, 0] : 0000 = 256 Mb 0001 = 512 Mb 0010 = 1 Gb 0011 = 2 Gb 0100 = 4 Gb 0101 = 8 Gb 0110 = 16 Gb All others reserved |

Byte 5: SDRAM Addressing

This byte describes the row addressing and the column addressing in the SDRAM device. Bits 2 ~ 0 encode the number of column address bits, and bits 5 ~ 3 encode the number of row address bits. These values come from the DDR3 SDRAM data sheet.

| Bits 7 ~ 6 | Bits 5 ~ 3 | Bits 2 ~ 0 |
|------------|--|---|
| Reserved | Row Address Bits | Column Address Bits |
| | Bit [5, 4, 3] : 000 = 12 001 = 13 010 = 14 011 = 15 100 = 16 All others reserved | Bit [2, 1, 0] : 000 = 9 001 = 10 010 = 11 011 = 12 All others reserved |

Byte 6: Module Nominal Voltage, VDD

This byte describes the Voltage Level for DRAM and other components on the module such as the register if applicable. Note that SPDs or thermal sensor components are on the VDDSPD supply and are not affected by this byte.

'Operable' is defined as the VDD voltage at which module operation is allowed using the performance values programmed in the SPD.

'Endurant' is defined as the VDD voltage at which the module may be powered without adversely affecting the life expectancy or reliability. Further specifications will exist to define the amount of time that the 'Endurant' voltage can be applied to the module. Operation is not supported at this voltage.

| Byte 6: Module Nominal Voltage, VDD | | | |
|---|---|---|---|
| Reserved | Module Minimum Nominal Voltage, VDD | | |
| Bit 7~3 | Bit 2 | Bit 1 | Bit 0 |
| Reserved | 0 = NOT 1.25 V operable 1 = 1.25 V operable | 0 = NOT 1.35 V operable 1 = 1.35 V operable | 0 = 1.5 V operable 1 = NOT 1.5 V operable |
| Note 1 1.35 V LV DDR3 devices are required to be 1.5 V operable. Note 2 All DDR3 devices are required to be 1.5 V endurant. Note 3 The value on Bit 0 uses a different polarity as compared to Bits 1 and 2 for backward compatibility with previous DDR3 SPD definitions. | | | |

Examples:

A value on bits 2~0 of 000 implies that the device supports nominal operable voltage of 1.5 V only.

A value on bits 2~0 of 010 implies that the device supports nominal operable voltages of 1.35 V and 1.5 V.

A value on bits 2~0 of 110 implies that the device supports nominal operable voltages of 1.25 V, 1.35 V, or 1.5 V.

A value on bits 2~0 of 111 implies that the device supports nominal operable voltages of 1.25 V or 1.35 V. The device is furthermore enduring to 1.5 V.

Byte 7: Module Organization

This byte describes the organization of the SDRAM module. Bits 2 ~ 0 encode the device width of the SDRAM devices. Bits 5 ~ 3 encode the number of physical ranks on the module. For example, for a double-rank module with x8 DRAMs, this byte is encoded 00 001 001, or 0x09.

| Bits 7 ~ 6 | Bits 5 ~ 3 | Bits 2 ~ 0 |
|------------|--|--|
| Reserved | Number of Ranks | SDRAM Device Width |
| | Bit [5, 4, 3] : 000 = 1 Rank 001 = 2 Ranks 010 = 3 Ranks 011 = 4 Ranks 100 = 8 Ranks All others reserved | Bit [2, 1, 0] : 000 = 4 bits 001 = 8 bits 010 = 16 bits 011 = 32 bits All others reserved |

Byte 8: Module Memory Bus Width

This byte describes the width of the SDRAM memory bus on the module. Bits 2 ~ 0 encode the primary bus width. Bits 4 ~ 3 encode the bus extensions such as parity or ECC.

| Bits 7 ~ 5 | Bits 4 ~ 3 | Bits 2 ~ 0 |
|------------|--|---|
| Reserved | Bus width extension, in bits | Primary bus width, in bits |
| | Bit [4, 3] : 000 = 0 bits (no extension) 001 = 8 bits All others reserved | Bit [2, 1, 0] : 000 = 8 bits 001 = 16 bits 010 = 32 bits 011 = 64 bits All others reserved |

Examples:

- 64 bit primary bus, no parity or ECC (64 bits total width): xxx 000 011
- 64 bit primary bus, with 8 bit ECC (72 bits total width): xxx 001 011

Calculating Module Capacity

The total memory capacity of the module may be calculated from SPD values. For example, to calculate the total capacity, in megabytes or gigabytes, of a typical module:

- $\text{SDRAM CAPACITY} \div 8 * \text{PRIMARY BUS WIDTH} \div \text{SDRAM WIDTH} * \text{RANKS}$

Release 24

where:

- SDRAM CAPACITY = SPD byte 4 bits 3~0
- PRIMARY BUS WIDTH = SPD byte 8 bits 2~0
- SDRAM WIDTH = SPD byte 7 bits 2~0
- RANKS = SPD byte 7 bits 5~3

Example: 2 ranks of 1 Gb SDRAMs with x4 organization on a module with a 64 bit primary bus:

- $1 \text{ Gb} \div 8 * 64 \div 4 * 2 = 4 \text{ GB}$

Example: 1 rank of 2 Gb SDRAMs with x8 organization on a module with a 64 bit primary bus:

- $2 \text{ Gb} \div 8 * 64 \div 8 * 1 = 2 \text{ GB}$

Commonly, parity or ECC are not counted in total module capacity, though they can also be included by adding the bus width extension in SPD byte 8 bits 4 ~ 3 to the primary bus width in the previous examples.

Byte 9: Fine Timebase (FTB) Dividend / Divisor

This byte defines a value in picoseconds that represents the fundamental timebase for fine grain timing calculations. This value is used as a multiplier for formulating subsequent timing parameters. The fine timebase (FTB) is defined as the fine timebase dividend, bits 7 ~ 4, divided by the fine timebase divisor, bits 3 ~ 0.

| Bits 7 ~ 4 | Bits 3 ~ 0 |
|------------------------------|-----------------------------|
| Fine Timebase (FTB) Dividend | Fine Timebase (FTB) Divisor |
| Values defined from 1 to 15 | Values defined from 1 to 15 |

Examples:

| Dividend | Divisor | Timebase (ps) | Use |
|----------|---------|---------------|---|
| 5 | 1 | 5 | When time granularity of 5 ps is required |
| 5 | 2 | 2.5 | When time granularity of 2.5 ps is required |
| 1 | 1 | 1 | When time granularity of 1 ps is required |

Byte 10: Medium Timebase (MTB) Dividend

Byte 11: Medium Timebase (MTB) Divisor

These bytes define a value in nanoseconds that represents the fundamental timebase for medium grain timing calculations. This value is typically the greatest common divisor for the range of clock frequencies (clock periods) supported by a particular SDRAM. This value is used as a multiplier for formulating subsequent timing parameters. The medium timebase (MTB) is defined as the medium timebase dividend (byte 10) divided by the medium timebase divisor (byte 11).

| Byte 10 Bits 7 ~ 0 | Byte 11 Bits 7 ~ 0 |
|--------------------------------|-------------------------------|
| Medium Timebase (MTB) Dividend | Medium Timebase (MTB) Divisor |
| Values defined from 1 to 255 | Values defined from 1 to 255 |

Examples:

| Dividend | Divisor | Timebase (ns) | Use |
|----------|----------|---------------|---|
| 1 | 8 (0x08) | 0.125 | For clock frequencies of 400 through 1066 MHz |

To simplify BIOS implementation, DIMMs associated with a given key byte value may differ in MTB value only by a factor of two. For DDR3 modules, the defined MTB values are:

| Dividend | Divisor | Timebase (ns) | Use |
|----------|-----------|---------------|-------------------------|
| 1 | 8 (0x08) | 0.125 | MTB Value for DDR3 |
| 1 | 16 (0x10) | 0.0625 | Reserved for future use |

Relating the MTB and FTB

When a timing value tXX cannot be expressed by an integer number of MTB units, the SPD must be encoded using both the MTB and FTB. The Fine Offsets are encoded using a two's complement value which, when multiplied by the FTB yields a positive or negative correction factor. Typically, for safety and for legacy compatibility, the MTB portion is rounded UP and the FTB correction is a negative value. The general algorithm for programming SPD values is:

```

Temp_val = tXX / MTB // Calculate as real number
Remainder = Temp_val modulo 1 // Determine if integer # MTBs
Fine_Correction = 1 - Remainder // If needed, what correction
if (Remainder == 0) then // Integer # MTBs?
    tXX(MTB) = Temp_val // Convert to integer
    tXX(FTB) = 0 // No correction needed
else // Needs correction
    tXX(MTB) = ceiling (Temp_val) // Round up for safety in legacy systems
    tXX(FTB) = Fine_Correction * MTB / FTB // Correction is negative offset
endif

```

To recalculate the value of tXX from the SPD values, a general formula BIOSes may use is:

$$tXX = tXX(MTB) * MTB + tXX(FTB) * FTB$$

Examples:

| tCKmin SPD Calculations Using MTB and FTB | | | |
|---|-------------------|-----------------------------------|-----------------------------------|
| Speed Bin | tCK Value Decimal | SPD byte 12 Decimal (Hexadecimal) | SPD byte 34 Decimal (Hexadecimal) |
| DDR3-1333 | 1.5 ns | 12 (0x0C) | 0 (0x00) |
| | = | (12 * 0.125) + (0 * 0.001) | |

| | | | |
|--|----------|-----------------------------|---------------|
| DDR3-1866 | 1.071 ns | 9 (0x09) | -54 (0xCA) |
| | = | (9 * 0.125) + (-54 * 0.001) | |
| Note: Examples assume MTB of 0.125 ns and FTB of 0.001 ns | | | |

Timing parameters using both MTB and FTB are:

TABLE 2.

| Parameter | MTB Byte(s) | FTB Byte |
|-----------|-------------|----------|
| tCKmin | 12 | 34 |
| tAmin | 16 | 35 |
| tRCDmin | 18 | 36 |
| tRPmin | 20 | 37 |
| tRCmin | 21, 23 | 38 |

The encoding of two's complement fine timebase offsets:

| Coding | | Value (Dec) | Value (Hex) | FTB Timebase | | |
|--------|----------|----------------|----------------|--------------|-----------|---------|
| Bit 7 | Bits 6~0 | | | 5 ps | 2.5 ps | 1 ps |
| 0 | 1111111 | +127 | 7F | +635 ps | +317.5 ps | +127 ps |
| 0 | 1111110 | +126 | 7E | +630 ps | +315 ps | +126 ps |
| ... | ... | ... | ... | | | |
| 0 | 0000001 | +1 | 01 | +5 ps | +2.5 ps | +1 ps |
| 0 | 0000000 | 0 | 00 | 0 | 0 | 0 |
| 1 | 1111111 | -1 | FF | -5 ps | -2.5 ps | -1 ps |
| 1 | 1111110 | -2 | FE | -10 ps | -5 ps | -2 ps |
| ... | ... | ... | ... | | | |
| 1 | 0000000 | -128 | 80 | -640 ps | -320 ps | -128 ps |

Rounding Algorithms

Software algorithms for calculation of timing parameters are subject to rounding errors from many sources. For example, a system may use a memory clock with a nominal frequency of 933.33... MHz, or a clock period of 1.0714... ns. Similarly, a system with a memory clock frequency of 1066.66... MHz yields mathematically a clock period of 0.9375... ns. In most cases, it is impossible to express all digits after the decimal point exactly, and rounding must be done because the SPD establishes a minimum granularity for timing parameters of 1 ps.

Rules for rounding must be defined to allow optimization of memory module performance without violating device parameters. These algorithms rely on results that are within guardbands on device testing and specification to avoid losing performance due to rounding errors.

These rules are:

1. Clock periods such as $t_{CKAVGmin}$ are rounded to the nearest picosecond of accuracy; for example, 0.9375... ns is rounded to 938 ps and 1.0714... ns is rounded to 1071 ps.
2. Parameters programmed in systems in numbers of clocks (nCK) but expressed in the SPD in units of time (ns or ps) are divided by the clock period, a guardband factor of 0.01 clocks is subtracted, then the result is rounded up to the nearest integer number of clocks. Examples:

| DDR3 Bin | Parameter | Value | @ $t_{CKAVGmin}$ | Temp Result | - Guardband | Rounding Result |
|--------------------|-----------|-------|------------------|-------------|-------------|-----------------|
| | | ps | ps | nCK | nCK | nCK |
| 1333 | t_{RRD} | 7500 | 1500 | 5.000 | 4.990 | 5 |
| 1866L | t_{RCD} | 12840 | 1071 | 11.988 | 11.978 | 12 |
| 1866M | t_{RC} | 47910 | 1071 | 44.733 | 44.724 | 45 |
| 1866M with downbin | t_{RC} | 47125 | 1071 | 44.001 | 43.991 | 44 |

Byte 12: SDRAM Minimum Cycle Time (t_{CKmin})

This byte defines the minimum cycle time for the SDRAM module, in medium timebase (MTB) units. This number applies to all applicable components on the module. This byte applies to SDRAM and support components as well as the overall capability of the DIMM. This value comes from the DDR3 SDRAM and support component data sheets.

| Bits 7 ~ 0 |
|---|
| Minimum SDRAM Cycle Time (t_{CKmin}) MTB Units |
| Values defined from 1 to 255 |

If t_{CKmin} cannot be divided evenly by the MTB, this byte must be rounded up to the next larger integer and the Fine Offset for t_{CKmin} (SPD byte 34) used for correction to get the actual value.

Examples:

| t_{CKmin} (MTB units) | MTB (ns) | t_{CKmin} Offset (FTB units) ¹ | FTB (ns) | t_{CKmin} Result (ns) | Use | |
|----------------------------|-------------|--|-------------|----------------------------|-------|----------------------------|
| 20 | 0x14 | 0.125 | 0 | 0.001 | 2.5 | DDR3-800 (400 MHz clock) |
| 15 | 0x0F | 0.125 | 0 | 0.001 | 1.875 | DDR3-1066 (533 MHz clock) |
| 12 | 0x0C | 0.125 | 0 | 0.001 | 1.5 | DDR3-1333 (667 MHz clock) |
| 10 | 0x0A | 0.125 | 0 | 0.001 | 1.25 | DDR3-1600 (800 MHz clock) |
| 9 | 0x09 | 0.125 | -54 | 0xCA | 1.071 | DDR3-1866 (933 MHz clock) |
| 8 | 0x08 | 0.125 | -62 | 0xC2 | 0.938 | DDR3-2133 (1067 MHz clock) |

Note 1 See SPD byte 34.

Byte 13: Reserved

Byte 14: CAS Latencies Supported, Least Significant Byte

Byte 15: CAS Latencies Supported, Most Significant Byte

These bytes define which CAS Latency (CL) values are supported. The range is from CL = 4 through CL = 18 with one bit per possible CAS Latency. A 1 in a bit position means that CL is supported, a 0 in that bit position means it is not supported. Since CL = 6 is required for all DDR3 speed bins, bit 2 of SPD byte 14 is always 1. These values come from

Release 24

the DDR3 SDRAM data sheet.

| Byte 14: CAS Latencies Supported, Low Byte | | | | | | | |
|---|---------|---------|---------|---------|---------|---------|---------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| CL = 11 | CL = 10 | CL = 9 | CL = 8 | CL = 7 | CL = 6 | CL = 5 | CL = 4 |
| 0 or 1 | 0 or 1 | 0 or 1 | 0 or 1 | 0 or 1 | 1 | 0 or 1 | 0 or 1 |
| Byte 15: CAS Latencies Supported, High Byte | | | | | | | |
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Reserved | CL = 18 | CL = 17 | CL = 16 | CL = 15 | CL = 14 | CL = 13 | CL = 12 |
| 0 | 0 or 1 | 0 or 1 | 0 or 1 | 0 or 1 | 0 or 1 | 0 or 1 | 0 or 1 |

Note 1 For each bit position, 0 means this CAS Latency is not supported, 1 means this CAS Latency is supported.

Example: DDR3-1600K

Byte 14 = 0xD4 (= 1101 0100) -- low byte.

Byte 15 = 0x00 (= 0000 0000) -- high byte.

| CAS Latencies | x | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 |
|---------------|---|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|
| CL Mask | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |

Results: Actual CAS Latencies supported = 6, 8, 10, and 11.

Byte 16: Minimum CAS Latency Time (t_{AAmin})

This byte defines the minimum CAS Latency in medium timebase (MTB) units. Software can use this information, along with the CAS Latencies supported (found in bytes 14 and 15) to determine the optimal cycle time for a particular module. This value comes from the DDR3 SDRAM data sheet.

| Bits 7 ~ 0 |
|---|
| Minimum SDRAM CAS Latency Time (t _{AAmin}) MTB Units |
| Values defined from 1 to 255 |

If t_{AAmin} cannot be divided evenly by the MTB, this byte must be rounded up to the next larger integer and the Fine Offset for t_{AAmin} (SPD byte 35) used for correction to get the actual value.

Examples:

| t _{AAmin} (MTB units) | MTB (ns) | t _{AAmin} Offset (FTB units) ¹ | FTB (ns) | t _{AAmin} Result (ns) | Use |
|-----------------------------------|-------------|---|-------------|-----------------------------------|---------------------------------|
| 100 | 0x64 | 0 | 0 | 0.001 | DDR3-800D |
| 120 | 0x78 | 0 | 0 | 0.001 | DDR3-800E |
| 90 | 0x5A | 0 | 0 | 0.001 | DDR3-1066E |
| 105 | 0x69 | 0 | 0 | 0.001 | DDR3-1066F |
| 120 | 0x78 | 0 | 0 | 0.001 | DDR3-1066G |
| 84 | 0x54 | 0 | 0 | 0.001 | DDR3-1333F |
| 96 | 0x60 | 0 | 0 | 0.001 | DDR3-1333G |
| 108 | 0x6C | 0 | 0 | 0.001 | DDR3-1333H ² |
| 105 | 0x69 | 0 | 0 | 0.001 | DDR3-1333H downbin ² |

| tAAmin (MTB units) | | MTB (ns) | tAAmin Offset (FTB units) ¹ | | FTB (ns) | tAAmin Result (ns) | Use |
|---|------|-------------|---|------|-------------|-----------------------|---------------------------------|
| 120 | 0x78 | 0.125 | 0 | 0 | 0.001 | 15 | DDR3-1333J |
| 80 | 0x50 | 0.125 | 0 | 0 | 0.001 | 10 | DDR3-1600G |
| 90 | 0x5A | 0.125 | 0 | 0 | 0.001 | 11.25 | DDR3-1600H |
| 100 | 0x64 | 0.125 | 0 | 0 | 0.001 | 12.5 | DDR3-1600J |
| 110 | 0x6E | 0.125 | 0 | 0 | 0.001 | 13.75 | DDR3-1600K ² |
| 105 | 0x69 | 0.125 | 0 | 0 | 0.001 | 13.125 | DDR3-1600K downbin ² |
| 86 | 0x56 | 0.125 | -50 | 0xCE | 0.001 | 10.7 | DDR3-1866J |
| 95 | 0x5F | 0.125 | -105 | 0x97 | 0.001 | 11.77 | DDR3-1866K |
| 103 | 0x67 | 0.125 | -35 | 0xDD | 0.001 | 12.84 | DDR3-1866L |
| 112 | 0x70 | 0.125 | -90 | 0xA6 | 0.001 | 13.91 | DDR3-1866M ² |
| 105 | 0x69 | 0.125 | 0 | 0 | 0.001 | 13.125 | DDR3-1866M downbin ² |
| 83 | 0x53 | 0.125 | -90 | 0xA6 | 0.001 | 10.285 | DDR3-2133K |
| 90 | 0x5A | 0.125 | -30 | 0xE2 | 0.001 | 11.22 | DDR3-2133L |
| 98 | 0x62 | 0.125 | -95 | 0xA1 | 0.001 | 12.155 | DDR3-2133M |
| 105 | 0x69 | 0.125 | -35 | 0xDD | 0.001 | 13.09 | DDR3-2133N |
| Note 1 See SPD byte 35. | | | | | | | |
| Note 2 Refer to device data sheet for downbin support details. | | | | | | | |

CAS Latency Calculation and Examples

CAS latency is not a purely analog value as DDR3 SDRAMs use the DLL to synchronize data and strobe outputs with the clock. All possible frequencies may not be tested, therefore an application should use the next smaller JEDEC standard tCKmin value (2.5, 1.875, 1.5, 1.25, 1.071, and 0.938 ns for DDR3 SDRAMs) when calculating CAS Latency. This section shows how the BIOS may calculate CAS latency based on Bytes 12 ~ 16, 34, and 35.

- Step 1: Determine the common set of supported CAS Latency values for all modules on the memory channel using the CAS Latencies Supported in SPD bytes 14 and 15.
- Step 2: Determine tAAmin(all) which is the largest tAAmin value for all modules on the memory channel (SPD bytes 16 and 35).
- Step 3: Determine tCKmin(all) which is the largest tCKmin value for all modules on the memory channel (SPD bytes 12 and 34).
- Step 4: For a proposed tCK value (tCKproposed) between tCKmin(all) and tCKmax, determine the desired CAS Latency. If tCKproposed is not a standard JEDEC value (2.5, 1.875, 1.5, 1.25, 1.071, or 0.938 ns) then tCKproposed must be adjusted to the next lower standard tCK value for calculating CLdesired.

$$CL_{\text{desired}} = \text{ceiling} (tAA_{\text{min}}(\text{all}) / tCK_{\text{proposed}})$$

where tAAmin is defined in Byte 16 and Byte 35. The ceiling function requires that the quotient be rounded up always.

- Step 5: Chose an actual CAS Latency (CLactual) that is greater than or equal to CLdesired and is supported by all modules on the memory channel as determined in step 1. If no such value exists, choose a higher tCKproposed value and repeat steps 4 and 5 until a solution is found.
- Step 6: Once the calculation of CLactual is completed, the BIOS must also verify that this CAS Latency value does not exceed tAAmax, which is 20 ns for all DDR3 speed grades, by multiplying CLactual times tCKproposed. If not, choose a lower CL value and repeat steps 5 and 6 until a solution is found.

Example 1: Slot 0 = DDR3-1066E 6-6-6, Slot 1 = DDR3-1333H 9-9-9

- Step 1: CL in slot 0 = 5, 6, 7, 8; CL in slot 1 = 6, 8, 9; Common CL = 6, 8
- Step 2: tAAmin in slot 0 = 11.25 ns; tAAmin in slot 1 = 13.5 ns; tAAmin(all) = 13.5 ns
- Step 3: tCKmin in slot 0 = 1.875 ns; tCKmin in slot 1 = 1.5 ns; tCKproposed = 1.875 ns
- Step 4: CLdesired = ceiling(13.5 / 1.875) = 8
- Step 5: CLactual = CLdesired
- Step 6: CLactual * tCKproposed = 8 * 1.875 = 15 < 20 ns ... value is okay
- Results: tCKactual = 1.875 ns, CLactual = 8

Example 2: Slot 0 = DDR3-800D 5-5-5, Slot 1 = DDR3-1066G 8-8-8

- Step 1: CL in slot 0 = 5, 6; CL in slot 1 = 6, 8; Common CL = 6
- Step 2: tAAmin in slot 0 = 12.5 ns; tAAmin in slot 1 = 15 ns; tAAmin(all) = 15 ns
- Step 3: tCKmin in slot 0 = 2.5 ns; tAAmin in slot 1 = 1.875 ns; tCKproposed = 2.5 ns
- Step 4: CLdesired = ceiling(15 / 2.5 ns) = 6
- Step 5: CLactual = CLdesired
- Step 6: CLactual * tCKproposed = 6 * 2.5 = 15 < 20 ns ... value is okay
- Results: tCKactual = 2.5 ns, CLactual = 6

Example 3: Slot 0 = DDR3-800D 5-5-5, Slot 1 = DDR3-1066G 8-8-8, System Bringup & Debug limits operating frequency to 333 MHz (tCK = 3.3 ns)

- Step 1: CL in slot 0 = 5, 6; CL in slot 1 = 6, 8; Common CL = 6
- Step 2: tAAmin in slot 0 = 12.5 ns; tAAmin in slot 1 = 15 ns; tAAmin(all) = 15 ns
- Step 3: tCKproposed = 3.3 ns
- Step 4: CLdesired = ceiling(15 / 3.3 ns) = 5
- Step 5: CLactual = 6
- Step 6: CLactual * tCKproposed = 6 * 3.3 = 19.8 < 20 ns ... value is okay
- Results: tCKactual = 3.3 ns, CLactual = 6

Byte 17: Minimum Write Recovery Time (t_{WRmin})

This byte defines the minimum SDRAM write recovery time in medium timebase (MTB) units. This value comes from the DDR3 SDRAM data sheet.

| |
|---|
| Bits 7 ~ 0 |
| Minimum Write Recovery Time (t_{WR}) |
| MTB Units |
| Values defined from 1 to 255 |

Example:

| t _{WRmin} (MTB units) | Timebase (ns) | t _{WR} Result (ns) | Use |
|-----------------------------------|------------------|--------------------------------|-----------------------|
| 120 | 0.125 | 15 | All DDR3 speed grades |

Step 1: The BIOS first determines the common operating frequency of all modules in the system, ensuring that the corresponding value of tCK (tCKactual) falls between tCKmin (Bytes 12 and 34) and tCKmax. If tCKactual is not a JEDEC standard value, the next smaller standard tCKmin value is used for calculating Write Recovery.

Step 2: The BIOS then calculates the “desired” Write Recovery (WRdesired):

$$WR_{desired} = \text{ceiling} (t_{WRmin} / t_{CKactual})$$

where tWR_{min} is defined in Byte 17. The ceiling function requires that the quotient be rounded up always.

Step 3: The BIOS then determines the “actual” Write Recovery (WR_{actual}):

$$WR_{actual} = \max(WR_{desired}, \min WR \text{ supported})$$

where min WR is the lowest Write Recovery supported by the DDR3 SDRAM. Note that not all WR values supported by DDR3 SDRAMs are sequential, so the next higher supported WR value must be used in some cases.

Usage example for DDR3-1333G operating at DDR3-1333:

$$\begin{aligned} tCK_{actual} &= 1.5 \text{ ns} \\ WR_{desired} &= 15 / 1.5 = 10 \\ WR_{actual} &= \max(10, 10) = 10 \end{aligned}$$

Byte 18: Minimum RAS# to CAS# Delay Time (t_{RCDmin})

This byte defines the minimum SDRAM RAS# to CAS# Delay in medium timebase (MTB) units. This value comes from the DDR3 SDRAM data sheet.

| |
|---|
| Bits 7 ~ 0 |
| Minimum RAS# to CAS# Delay (t_{RCD}) MTB Units |
| Values defined from 1 to 255 |

If t_{RCDmin} cannot be divided evenly by the MTB, this byte must be rounded up to the next larger integer and the Fine Offset for t_{RCDmin} (SPD byte 36) used for correction to get the actual value.

Examples:

| tRCD (MTB units) | MTB (ns) | tRCD Offset (FTB units) ¹ | FTB (ns) | tRCD Result (ns) | Use | | |
|------------------|----------|--------------------------------------|----------|------------------|-------|--------|---------------------------------|
| 100 | 0x64 | 0.125 | 0 | 0 | 0.001 | 12.5 | DDR3-800D |
| 120 | 0x78 | 0.125 | 0 | 0 | 0.001 | 15 | DDR3-800E |
| 90 | 0x5A | 0.125 | 0 | 0 | 0.001 | 11.25 | DDR3-1066E |
| 105 | 0x69 | 0.125 | 0 | 0 | 0.001 | 13.125 | DDR3-1066F |
| 120 | 0x78 | 0.125 | 0 | 0 | 0.001 | 15 | DDR3-1066G |
| 84 | 0x54 | 0.125 | 0 | 0 | 0.001 | 10.5 | DDR3-1333F |
| 96 | 0x60 | 0.125 | 0 | 0 | 0.001 | 12 | DDR3-1333G |
| 108 | 0x6C | 0.125 | 0 | 0 | 0.001 | 13.5 | DDR3-1333H ² |
| 105 | 0x69 | 0.125 | 0 | 0 | 0.001 | 13.125 | DDR3-1333H downbin ² |
| 120 | 0x78 | 0.125 | 0 | 0 | 0.001 | 15 | DDR3-1333J |
| 80 | 0x50 | 0.125 | 0 | 0 | 0.001 | 10 | DDR3-1600G |
| 90 | 0x5A | 0.125 | 0 | 0 | 0.001 | 11.25 | DDR3-1600H |
| 100 | 0x64 | 0.125 | 0 | 0 | 0.001 | 12.5 | DDR3-1600J |
| 110 | 0x6E | 0.125 | 0 | 0 | 0.001 | 13.75 | DDR3-1600K ² |
| 105 | 0x69 | 0.125 | 0 | 0 | 0.001 | 13.125 | DDR3-1600K downbin ² |
| 86 | 0x56 | 0.125 | -50 | 0xCE | 0.001 | 10.7 | DDR3-1866J |
| 95 | 0x5F | 0.125 | -105 | 0x97 | 0.001 | 11.77 | DDR3-1866K |
| 103 | 0x67 | 0.125 | -35 | 0xDD | 0.001 | 12.84 | DDR3-1866L |
| 112 | 0x70 | 0.125 | -90 | 0xA6 | 0.001 | 13.91 | DDR3-1866M ² |
| 105 | 0x69 | 0.125 | 0 | 0 | 0.001 | 13.125 | DDR3-1866M downbin ² |
| 83 | 0x53 | 0.125 | -90 | 0xA6 | 0.001 | 10.285 | DDR3-2133K |

| tRCD (MTB units) | | MTB (ns) | tRCD Offset (FTB units) ¹ | | FTB (ns) | tRCD Result (ns) | Use |
|---------------------|------|-------------|---|------|-------------|---------------------|------------|
| 90 | 0x5A | 0.125 | -30 | 0xE2 | 0.001 | 11.22 | DDR3-2133L |
| 98 | 0x62 | 0.125 | -95 | 0xA1 | 0.001 | 12.155 | DDR3-2133M |
| 105 | 0x69 | 0.125 | -35 | 0xDD | 0.001 | 13.09 | DDR3-2133N |

Note 1 See SPD byte 36.
Note 2 Refer to device data sheet for downbin support details.

Byte 19: Minimum Row Active to Row Active Delay Time (t_{RRDmin})

This byte defines the minimum SDRAM Row Active to Row Active Delay Time in medium timebase units. This value comes from the DDR3 SDRAM data sheet. The value of this number may be dependent on the SDRAM page size; please refer to the DDR3 SDRAM data sheet section on Addressing to determine the page size for these devices. Controller designers must also note that at some frequencies, a minimum number of clocks may be required resulting in a larger t_{RRDmin} value than indicated in the SPD. For example, t_{RRDmin} for DDR3-800 must be 4 clocks.

| Bits 7 ~ 0 |
|---|
| Minimum Row Active to Row Active Delay (t_{RRD}) MTB Units |
| Values defined from 1 to 255 |

Examples:

| tRRD (MTB units) | Timebase (ns) | tRRD Result (ns) | Use |
|---------------------|------------------|---------------------|-----------------------------------|
| 48 | 0.125 | 6.0 | Example: DDR3-1333, 1KB page size |
| 60 | 0.125 | 7.5 | Example: DDR3-1333, 2KB page size |
| 80 | 0.125 | 10 | Example: DDR3-800, 1KB page size |

Note 1 tRRD is at least 4 nCK independent of operating frequency.

Byte 20: Minimum Row Precharge Delay Time (t_{RPmin})

This byte defines the minimum SDRAM Row Precharge Delay Time in medium timebase (MTB) units. This value comes from the DDR3 SDRAM data sheet.

| Bits 7 ~ 0 |
|--|
| Minimum Row Precharge Time (t_{RP}) MTB Units |
| Values defined from 1 to 255 |

If t_{RPmin} cannot be divided evenly by the MTB, this byte must be rounded up to the next larger integer and the Fine Offset for t_{RPmin} (SPD byte 37) used for correction to get the actual value.

Examples:

| tRP (MTB units) | | MTB (ns) | tRP Offset (FTB units) ¹ | | FTB (ns) | tRP Result (ns) | Use |
|--------------------|------|-------------|--|---|-------------|--------------------|------------|
| 100 | 0x64 | 0.125 | 0 | 0 | 0.001 | 12.5 | DDR3-800D |
| 120 | 0x78 | 0.125 | 0 | 0 | 0.001 | 15 | DDR3-800E |
| 90 | 0x5A | 0.125 | 0 | 0 | 0.001 | 11.25 | DDR3-1066E |

| tRP (MTB units) | | MTB (ns) | tRP Offset (FTB units) ¹ | | FTB (ns) | tRP Result (ns) | Use |
|--------------------|------|-------------|--|------|-------------|--------------------|---------------------------------|
| 105 | 0x69 | 0.125 | 0 | 0 | 0.001 | 13.125 | DDR3-1066F |
| 120 | 0x78 | 0.125 | 0 | 0 | 0.001 | 15 | DDR3-1066G |
| 84 | 0x54 | 0.125 | 0 | 0 | 0.001 | 10.5 | DDR3-1333F |
| 96 | 0x60 | 0.125 | 0 | 0 | 0.001 | 12 | DDR3-1333G |
| 108 | 0x6C | 0.125 | 0 | 0 | 0.001 | 13.5 | DDR3-1333H ² |
| 105 | 0x69 | 0.125 | 0 | 0 | 0.001 | 13.125 | DDR3-1333H downbin ² |
| 120 | 0x78 | 0.125 | 0 | 0 | 0.001 | 15 | DDR3-1333J |
| 80 | 0x50 | 0.125 | 0 | 0 | 0.001 | 10 | DDR3-1600G |
| 90 | 0x5A | 0.125 | 0 | 0 | 0.001 | 11.25 | DDR3-1600H |
| 100 | 0x64 | 0.125 | 0 | 0 | 0.001 | 12.5 | DDR3-1600J |
| 110 | 0x6E | 0.125 | 0 | 0 | 0.001 | 13.75 | DDR3-1600K ² |
| 105 | 0x69 | 0.125 | 0 | 0 | 0.001 | 13.125 | DDR3-1600K downbin ² |
| 86 | 0x56 | 0.125 | -50 | 0xCE | 0.001 | 10.7 | DDR3-1866J |
| 95 | 0x5F | 0.125 | -105 | 0x97 | 0.001 | 11.77 | DDR3-1866K |
| 103 | 0x67 | 0.125 | -35 | 0xDD | 0.001 | 12.84 | DDR3-1866L |
| 112 | 0x70 | 0.125 | -90 | 0xA6 | 0.001 | 13.91 | DDR3-1866M ² |
| 105 | 0x69 | 0.125 | 0 | 0 | 0.001 | 13.125 | DDR3-1866M downbin ² |
| 83 | 0x53 | 0.125 | -90 | 0xA6 | 0.001 | 10.285 | DDR3-2133K |
| 90 | 0x5A | 0.125 | -30 | 0xE2 | 0.001 | 11.22 | DDR3-2133L |
| 98 | 0x62 | 0.125 | -95 | 0xA1 | 0.001 | 12.155 | DDR3-2133M |
| 105 | 0x69 | 0.125 | -35 | 0xDD | 0.001 | 13.09 | DDR3-2133N |

Note 1 See SPD byte 37.

Note 2 Refer to device data sheet for downbin support details.

Byte 21: Upper Nibbles for t_{RAS} and t_{RC}

This byte defines the most significant nibbles for the values of t_{RAS} (byte 22) and t_{RC} (byte 23). These values come from the DDR3 SDRAM data sheet.

| Bits 7 ~ 4 | Bits 3 ~ 0 |
|---|--|
| t _{RC} Most Significant Nibble | t _{RAS} Most Significant Nibble |
| See Byte 23 description | See Byte 22 description |

Byte 22: Minimum Active to Precharge Delay Time (t_{RASmin}), Least Significant Byte

The lower nibble of Byte 21 and the contents of Byte 22 combined create a 12-bit value which defines the minimum SDRAM Active to Precharge Delay Time in medium timebase (MTB) units. The most significant bit is Bit 3 of Byte 21, and the least significant bit is Bit 0 of Byte 22. This value comes from the DDR3 SDRAM data sheet.

| Byte 21 Bits 3 ~ 0, Byte 22 Bits 7 ~ 0 |
|---|
| Minimum Active to Precharge Time (t _{RAS}) MTB Units |
| Values defined from 1 to 4095 |

Examples:

| t _{RAS} (MTB units) | MTB (ns) | t _{RAS} Result (ns) | Use |
|---------------------------------|-------------|---------------------------------|-----------|
| 300 | 0x12C | 37.5 | DDR3-800D |

| tRAS (MTB units) | | MTB (ns) | tRAS Result (ns) | Use |
|---------------------|-------|-------------|---------------------|------------|
| 300 | 0x12C | 0.125 | 37.5 | DDR3-800E |
| 300 | 0x12C | 0.125 | 37.5 | DDR3-1066E |
| 300 | 0x12C | 0.125 | 37.5 | DDR3-1066F |
| 300 | 0x12C | 0.125 | 37.5 | DDR3-1066G |
| 288 | 0x120 | 0.125 | 36 | DDR3-1333F |
| 288 | 0x120 | 0.125 | 36 | DDR3-1333G |
| 288 | 0x120 | 0.125 | 36 | DDR3-1333H |
| 288 | 0x120 | 0.125 | 36 | DDR3-1333J |
| 280 | 0x118 | 0.125 | 35 | DDR3-1600G |
| 280 | 0x118 | 0.125 | 35 | DDR3-1600H |
| 280 | 0x118 | 0.125 | 35 | DDR3-1600J |
| 280 | 0x118 | 0.125 | 35 | DDR3-1600K |
| 272 | 0x110 | 0.125 | 34 | DDR3-1866J |
| 272 | 0x110 | 0.125 | 34 | DDR3-1866K |
| 272 | 0x110 | 0.125 | 34 | DDR3-1866L |
| 272 | 0x110 | 0.125 | 34 | DDR3-1866M |
| 264 | 0x108 | 0.125 | 33 | DDR3-2133K |
| 264 | 0x108 | 0.125 | 33 | DDR3-2133L |
| 264 | 0x108 | 0.125 | 33 | DDR3-2133M |
| 264 | 0x108 | 0.125 | 33 | DDR3-2133N |

Byte 23: Minimum Active to Active/Refresh Delay Time (t_{RCmin}), Least Significant Byte

The upper nibble of Byte 21 and the contents of Byte 23 combined create a 12-bit value which defines the minimum SDRAM Active to Active/Refresh Delay Time in medium timebase (MTB) units. The most significant bit is Bit 7 of Byte 21, and the least significant bit is Bit 0 of Byte 23. This value comes from the DDR3 SDRAM data sheet.

| Byte 21 Bits 7 ~ 4, Byte 23 Bits 7 ~ 0 |
|---|
| Minimum Active to Active/Refresh Time (t_{RC}) MTB Units |
| Values defined from 1 to 4095 |

If t_{RCmin} cannot be divided evenly by the MTB, this byte must be rounded up to the next larger integer and the Fine Offset for t_{RCmin} (SPD byte 38) used for correction to get the actual value.

Examples:

| tRC (MTB units) | MTB (ns) | tRC Offset (FTB units) ¹ | FTB (ns) | tRC Result (ns) | Use | |
|--------------------|-------------|--|-------------|--------------------|--------|---------------------------------|
| 400 | 0x190 | 0 | 0 | 0.001 | 50 | DDR3-800D |
| 420 | 0x1A4 | 0 | 0 | 0.001 | 52.5 | DDR3-800E |
| 390 | 0x186 | 0 | 0 | 0.001 | 48.75 | DDR3-1066E |
| 405 | 0x195 | 0 | 0 | 0.001 | 50.625 | DDR3-1066F |
| 420 | 0x1A4 | 0 | 0 | 0.001 | 52.5 | DDR3-1066G |
| 372 | 0x174 | 0 | 0 | 0.001 | 46.5 | DDR3-1333F |
| 384 | 0x180 | 0 | 0 | 0.001 | 48 | DDR3-1333G |
| 396 | 0x18C | 0 | 0 | 0.001 | 49.5 | DDR3-1333H ² |
| 393 | 0x189 | 0 | 0 | 0.001 | 49.125 | DDR3-1333H downbin ² |
| 408 | 0x198 | 0 | 0 | 0.001 | 51 | DDR3-1333J |
| 360 | 0x168 | 0 | 0 | 0.001 | 45 | DDR3-1600G |
| 370 | 0x172 | 0 | 0 | 0.001 | 46.25 | DDR3-1600H |

| tRC (MTB units) | | MTB (ns) | tRC Offset (FTB units) ¹ | | FTB (ns) | tRC Result (ns) | Use |
|--------------------|-------|-------------|--|------|-------------|--------------------|---------------------------------|
| 380 | 0x17C | 0.125 | 0 | 0 | 0.001 | 47.5 | DDR3-1600J |
| 390 | 0x186 | 0.125 | 0 | 0 | 0.001 | 48.75 | DDR3-1600K ² |
| 385 | 0x181 | 0.125 | 0 | 0 | 0.001 | 48.125 | DDR3-1600K downbin ² |
| 358 | 0x166 | 0.125 | -50 | 0xCE | 0.001 | 44.7 | DDR3-1866J |
| 367 | 0x16F | 0.125 | -105 | 0x97 | 0.001 | 45.77 | DDR3-1866K |
| 375 | 0x177 | 0.125 | -35 | 0xDD | 0.001 | 46.84 | DDR3-1866L |
| 384 | 0x180 | 0.125 | -90 | 0xA6 | 0.001 | 47.91 | DDR3-1866M ² |
| 377 | 0x179 | 0.125 | 0 | 0 | 0.001 | 47.125 | DDR3-1866M downbin ² |
| 347 | 0x15B | 0.125 | -90 | 0xA6 | 0.001 | 43.285 | DDR3-2133K |
| 354 | 0x162 | 0.125 | -30 | 0xE2 | 0.001 | 44.22 | DDR3-2133L |
| 362 | 0x16A | 0.125 | -95 | 0xA1 | 0.001 | 45.155 | DDR3-2133M |
| 369 | 0x171 | 0.125 | -35 | 0xDD | 0.001 | 46.09 | DDR3-2133N |

Note 1 See SPD byte 38.

Note 2 Refer to device data sheet for downbin support details.

Byte 24: Minimum Refresh Recovery Delay Time (t_{RFCmin}), Least Significant Byte

Byte 25: Minimum Refresh Recovery Delay Time (t_{RFCmin}), Most Significant Byte

The contents of Byte 24 and the contents of Byte 25 combined create a 16-bit value which defines the minimum SDRAM Refresh Recovery Time Delay in medium timebase (MTB) units. The most significant bit is Bit 7 of Byte 25, and the least significant bit is Bit 0 of Byte 24. These values come from the DDR3 SDRAM data sheet.

| Byte 25 Bits 7 ~ 0, Byte 24 Bits 7 ~ 0 |
|---|
| Minimum Refresh Recover Time Delay (t_{RFC}) MTB Units |
| Values defined from 1 to 65535 |

Examples:

| tRFC (MTB units) | | Timebase (ns) | tRFC Result (ns) | Use |
|---------------------|-------|------------------|---------------------|--------|
| 720 | 0x2D0 | 0.125 | 90 | 512 Mb |
| 880 | 0x370 | 0.125 | 110 | 1 Gb |
| 1280 | 0x500 | 0.125 | 160 | 2 Gb |
| 2400 | 0x960 | 0.125 | 300 | 4 Gb |
| 2800 | 0xAF0 | 0.125 | 350 | 8 Gb |

Byte 26: Minimum Internal Write to Read Command Delay Time (t_{WTRmin})

This byte defines the minimum SDRAM Internal Write to Read Delay Time in medium timebase (MTB) units. This value comes from the DDR3 SDRAM data sheet. The value of this number may be dependent on the SDRAM page size; please refer to the DDR3 SDRAM data sheet section on Addressing to determine the page size for these devices. Controller designers must also note that at some frequencies, a minimum number of clocks may be required resulting in a larger t_{WTRmin} value than indicated in the SPD. For example, t_{WTRmin} for DDR3-800 must be 4 clocks.

| |
|---|
| Bits 7 ~ 0 |
| Internal Write to Read Delay Time (t_{WTR}) MTB Units |
| Values defined from 1 to 255 |

Examples:

| tWTR (MTB units) | | Timebase (ns) | tWTR Result (ns) | Use |
|-----------------------------|------|--------------------------|-----------------------------|---------------------------|
| 60 | 0x3C | 0.125 | 7.5 | All DDR3 SDRAM speed bins |

Note 1 tWTR is at least 4 nCK independent of operating frequency.

Byte 27: Minimum Internal Read to Precharge Command Delay Time (t_{RTPmin})

This byte defines the minimum SDRAM Internal Read to Precharge Delay Time in medium timebase (MTB) units. This value comes from the DDR3 SDRAM data sheet. The value of this number may be dependent on the SDRAM page size; please refer to the DDR3 SDRAM data sheet section on Addressing to determine the page size for these devices. Controller designers must also note that at some frequencies, a minimum number of clocks may be required resulting in a larger tRTPmin value than indicated in the SPD. For example, tRTPmin for DDR3-800 must be 4 clocks.

| |
|---|
| Bits 7 ~ 0 |
| Internal Read to Precharge Delay Time (t_{RTP}) MTB Units |
| Values defined from 1 to 255 |

Examples:

| tRTP (MTB units) | | Timebase (ns) | tRTP Result (ns) | Use |
|-----------------------------|------|--------------------------|-----------------------------|---------------------------|
| 60 | 0x3C | 0.125 | 7.5 | All DDR3 SDRAM speed bins |

Note 1 tRTP is at least 4 nCK independent of operating frequency.

Byte 28: Upper Nibble for t_{FAW}

This byte defines the most significant nibble for the value of tFAW (SPD byte 29). This value comes from the DDR3 SDRAM data sheet.

| Bits 7 ~ 4 | Bits 3 ~ 0 |
|-------------------|---|
| Reserved | t_{FAW} Most Significant Nibble |
| Reserved | See Byte 29 description |

Byte 29: Minimum Four Activate Window Delay Time (t_{FAWmin}), Least Significant Byte

The lower nibble of Byte 28 and the contents of Byte 29 combined create a 12-bit value which defines the minimum SDRAM Four Activate Window Delay Time in medium timebase (MTB) units. This value comes from the DDR3 SDRAM data sheet. The value of this number may be dependent on the SDRAM page size; please refer to the DDR3 SDRAM data sheet section on Addressing to determine the page size for these devices.

| |
|--|
| Byte 28 Bits 3 ~ 0, Byte 29 Bits 7 ~ 0 |
| Minimum Four Activate Window Delay Time (t_{FAW}) MTB Units |
| Values defined from 1 to 4095 |

Examples:

| tFAW (MTB units) | | Timebase (ns) | tFAW Result (ns) | Use |
|---------------------|-------|------------------|---------------------|------------------------------------|
| 320 | 0x140 | 0.125 | 40 | Example: DDR3-800, 1 KB page size |
| 400 | 0x190 | 0.125 | 50 | Example: DDR3-800, 2 KB page size |
| 300 | 0x12C | 0.125 | 37.5 | Example: DDR3-1066, 1 KB page size |
| 400 | 0x190 | 0.125 | 50 | Example: DDR3-1066, 2 KB page size |
| 240 | 0x0F0 | 0.125 | 30 | Example: DDR3-1333, 1 KB page size |
| 360 | 0x168 | 0.125 | 45 | Example: DDR3-1333, 2 KB page size |
| 240 | 0x0F0 | 0.125 | 30 | Example: DDR3-1600, 1 KB page size |
| 320 | 0x140 | 0.125 | 40 | Example: DDR3-1600, 2 KB page size |
| 216 | 0x0D8 | 0.125 | 27 | Example: DDR3-1866, 1 KB page size |
| 280 | 0x118 | 0.125 | 35 | Example: DDR3-1866, 2 KB page size |
| 200 | 0x0C8 | 0.125 | 25 | Example: DDR3-2133, 1 KB page size |
| 280 | 0x118 | 0.125 | 35 | Example: DDR3-2133, 2 KB page size |

Byte 30: SDRAM Optional Features

This byte defines support for certain SDRAM features and the optional drive strengths supported by the SDRAMs on this module. This value comes from the DDR3 SDRAM data sheet.

| Bit 7 | Bits 6 ~ 2 | Bit 1 | Bit 0 |
|------------------------------------|-----------------|------------------------------------|------------------------------------|
| DLL-Off Mode Support | Reserved | RZQ / 7 | RZQ / 6 |
| 0 = Not Supported 1 = Supported | | 0 = Not Supported 1 = Supported | 0 = Not Supported 1 = Supported |

Byte 31: SDRAM Thermal and Refresh Options

This byte describes the module's supported operating temperature ranges and refresh options. These values come from the DDR3 SDRAM data sheet. Use of self refresh in the Extended Temperature Range, ASR or ODTS require appropriate SDRAM Mode Register programming (MR2 bits A6, A7, and MR3 bit A3). Please refer to the DDR3 SDRAM data sheet (JESD79-3 or supplier data sheet) for a complete description of these options.

| Bit 7 | Bits 6 ~ 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--|-----------------|--|---|--|---|
| Partial Array Self Refresh (PASR) | Reserved | On-die Thermal Sensor (ODTS) Readout | Auto Self Refresh (ASR) | Extended Temperature Refresh Rate | Extended Temperature Range |
| 1 = Supported 0 = Not supported | | 1 = On-die thermal sensor readout is supported 0 = On-die thermal sensor readout is not supported (pending ballot of ODTS) | 1 = ASR is supported and the SDRAM will determine the proper refresh rate for any supported temperature 0 = ASR is not supported | 1 = Extended operating temperature range from 85-95 °C supported with standard 1X refresh rate 0 = Use in extended operating temperature range from 85-95 °C requires 2X refresh rate | 1 = Normal and extended operating temperature range 0-95 °C supported 0 = Normal operating temperature range 0-85 °C supported |

Examples:

If SPD Byte 31 bit 0 = 0, the SDRAM does not support extended temperature range use and the SDRAM MR2 bit A7 must be set to 0. 1X refresh rate across the normal temperature range of 0-85 °C is supported.

If SPD Byte 31 bit 0 = 1, then the extended temperature range from 85-95 °C is supported and the SDRAM MR2 bit A7 may be set to 1. SPD byte 31 bit 1 may be used to determine an appropriate refresh rate when operating in the extended temperature range.

If SPD Byte 31 bit 2 = 0, then the SDRAM MR2 bit A6 must be set to 0. SDRAM MR2 bit A7 must be programmed to indicate the temperature range (TOPER) for subsequent self refresh operation.

If SPD Byte 31 bit 3 = 1, the on-die thermal sense logic can be used in conjunction with SPD Byte 31 bits 0 and 1 to determine an appropriate refresh rate and/or monitor the maximum operating temperature.

Byte 32: Module Thermal Sensor

This byte describes the module's supported thermal options.

| Bit 7 | Bits 6 ~ 0 |
|--|---|
| Thermal Sensor¹ | Thermal Sensor Accuracy |
| 0 = Thermal sensor not incorporated onto this assembly 1 = Thermal sensor incorporated onto this assembly | 0 = Undefined All others settings to be defined. |
| Note 1 Thermal sensor compliant with TSE2002 specifications. | |

Byte 33: SDRAM Device Type

This byte describes the type of SDRAM Device on the module.

| Bit 7 | Bits 6~4 | Bits 3~2 | Bit 1~0 |
|---|---|---------------|--|
| SDRAM Device Type | Die Count | Reserved | Signal Loading ² |
| 0 = Standard Monolithic DRAM Device 1 = Non-Standard Device ¹ | 000 = Not specified 001 = Single die 010 = 2 die 011 = 4 die 100 = 8 die All others settings reserved. | 0 = Undefined | 00 = Not specified 01 = Multi load stack 10 = Single load stack 11 = Reserved |
| <p>Note 1 This includes Dual Die, Quad Die, Multi-Die and Physical stacked devices - anything that is outside the standard monolithic device.</p> <p>Note 2 Refers to loading on signals at SDRAM balls. Loading on certain signals (CKE, ODT, etc.) per specification of device stacking as defined in JESD79-3.</p> | | | |

Byte 34: Fine Offset for SDRAM Minimum Cycle Time (tCKmin)

This byte modifies the calculation of SPD Byte 12 (MTB units) with a fine correction using FTB units. The value of tCKmin comes from the SDRAM data sheet. This value is a two's complement multiplier for FTB units, ranging from +127 to -128.

Examples: See SPD byte 12. For Two's Complement encoding, see **Relating the MTB and FTB**.

Byte 35: Fine Offset for Minimum CAS Latency Time (tAmin)

This byte modifies the calculation of SPD Byte 16 (MTB units) with a fine correction using FTB units. The value of tAmin comes from the SDRAM data sheet. This value is a two's complement multiplier for FTB units, ranging from +127 to -128.

Examples: See SPD Byte 16. For Two's Complement encoding, see **Relating the MTB and FTB**.

Byte 36: Fine Offset for Minimum RAS# to CAS# Delay Time (tRCDmin)

This byte modifies the calculation of SPD Byte 18 (MTB units) with a fine correction using FTB units. The value of tRCDmin comes from the SDRAM data sheet. This value is a two's complement multiplier for FTB units, ranging from +127 to -128.

Examples: See SPD byte 18. For Two's Complement encoding, see **Relating the MTB and FTB**.

Byte 37: Minimum Row Precharge Delay Time (tRPmin)

This byte modifies the calculation of SPD Byte 20 (MTB units) with a fine correction using FTB units. The value of tRPmin comes from the SDRAM data sheet. This value is a two's complement multiplier for FTB units, ranging from +127 to -128.

Examples: See SPD byte 20. For Two's Complement encoding, see **Relating the MTB and FTB**.

Byte 38: Fine Offset for Minimum Active to Active/Refresh Delay Time (tRCmin)

This byte modifies the calculation of SPD Bytes 21 and 23 (MTB units) with a fine correction using FTB units. The value of tRCmin comes from the SDRAM data sheet. This value is a two's complement multiplier for FTB units, ranging from +127 to -128.

Examples: See SPD byte 21 and 23. For Two's Complement encoding, see **Relating the MTB and FTB**.

Byte 39 ~ 40: Reserved, General Section

Byte 41: SDRAM Maximum Active Count (MAC) Value

This byte describes the SDRAM Maximum Activate Count and the Maximum Activate Window. Bits 7~6 may have system implications; contacting the DRAM supplier for guidance is required.

| Bits 7~6 | Bits 5~4 | Bits 3~0 |
|--|--|--|
| Vendor Specific | Maximum Activate Window (tMAW) | Maximum Activate Count (MAC) |
| Contact DRAM supplier for guidance in coding or interpreting these bits | Bits [5, 4]: 00 = 8192 * tREFI 01 = 4096 * tREFI 10 = 2048 * tREFI 11 = Reserved | Bits [3, 2, 1, 0] : 0000 = Untested MAC ¹ 0001 = 700 K 0010 = 600 K 0011 = 500 K 0100 = 400 K 0101 = 300 K 0110 = 200 K 0111 = Reserved 1000 = Unrestricted MAC ² All other codes reserved |
| Note 1 Untested MAC means the device is not tested for tMAW and/or MAC; no particular value should be assumed. Note 2 Unrestricted MAC means there is no restriction to the number of activates to a given row in a refresh period providing DRAM timing requirements such as tRCmin and refresh requirements are not violated. | | |

Byte 42 ~ 59: Reserved, General Section

2.2 Module-Specific Section: Bytes 60 ~ 116

The content of bytes 60~116 of this SPD are determined according to specific DDR3 module families. Module Type Key Byte 3 is used as an index for the encoding of bytes 60 ~ 116. The content of bytes 60 ~ 116 are described in multiple subsections, one for each memory module family.

At the end of this Annex there are four separate subsections—one for each DDR3 module family—that define the bytes in SPD locations 60~116. These module families and their respective subsections are:

- Annex K.1: Unbuffered Memory Modules
- Annex K.2: Registered Memory Modules
- Annex K.3: Clocked Memory Modules
- Annex K.4: Load Reduced Memory Modules

2.3 Unique Module ID: Bytes 117 ~ 125

Byte 117: Module Manufacturer ID Code, Least Significant Byte

Byte 118: Module Manufacturer ID Code, Most Significant Byte

This two-byte field indicates the manufacturer of the module, encoded as follows: the first byte is the number of continuation bytes indicated in JEP-106; the second byte is the last non-zero byte of the manufacturer's ID code, again as indicated in JEP-106.

| Byte 118, Bits 7 ~ 0 | Byte 117, Bit 7 | Byte 117, Bits 6 ~ 0 |
|---|-------------------------------------|---|
| Last non-zero byte, Module Manufacturer | Odd Parity for Byte 117, bits 6 ~ 0 | Number of continuation codes, Module Manufacturer |
| See JEP-106 | | See JEP-106 |

Examples:

| Company | JEP-106 | | # continuation codes | SPD | |
|------------|---------|------|----------------------|----------|----------|
| | Bank | Code | | Byte 117 | Byte 118 |
| Fujitsu | 1 | 04 | 0 | 0x80 | 0x04 |
| US Modular | 5 | A8 | 4 | 0x04 | 0xA8 |

Byte 119: Module Manufacturing Location

The module manufacturer includes an identifier that uniquely defines the manufacturing location of the memory module. While the SPD spec will not attempt to present a decode table for manufacturing sites, the individual manufacturer may keep track of manufacturing location and its appropriate decode represented in this byte.

Bytes 120 ~ 121: Module Manufacturing Date

The module manufacturer includes a date code for the module. The JEDEC definitions for bytes 120 and 121 are year and week respectively. These bytes must be represented in Binary Coded Decimal (BCD). For example, week 47 in year 2003 would be coded as 0x03 (0000 0011) in byte 120 and 0x47 (0100 0111) in byte 121.

Bytes 122 ~ 125: Module Serial Number

The supplier must include a unique serial number for the module. The supplier may use whatever decode method desired to maintain a unique serial number for each module.

One method of achieving this is by assigning a byte in the field from 122 ~ 125 as a tester ID byte and using the remaining bytes as a sequential serial number. Bytes 117 ~ 125 will then result in a nine-byte unique module identifier. Note that part number is not included in this identifier: the supplier may not give the same value for Bytes 119 ~ 125 to more than one DIMM even if the DIMMs have different part numbers.

2.4 CRC: Bytes 126 ~ 127

Bytes 126 ~ 127: SPD Cyclical Redundancy Code (CRC)

This two-byte field contains the calculated CRC for previous bytes in the SPD. The following algorithm and data structures (shown in C) are to be followed in calculating and checking the code. Bit 7 of Byte 0 indicates which bytes are covered by the CRC.

```
int Crc16 (char *ptr, int count)
{
    int crc, i;

    crc = 0;
    while (--count >= 0) {
        crc = crc ^ (int)*ptr++ << 8;
        for (i = 0; i < 8; ++i)
            if (crc & 0x8000)
                crc = crc << 1 ^ 0x1021;
            else
                crc = crc << 1;
    }
    return (crc & 0xFFFF);
}
```

```
char spdBytes[] = { SPD_byte_0, SPD_byte_1, ..., SPD_byte_N-1 };
int data16;
```

```
data16 = Crc16 (spdBytes, sizeof(spdBytes));
SPD_byte_126 = (char) (data16 & 0xFF);
SPD_byte_127 = (char) (data16 >> 8);
```

2.5 Other Manufacturer Fields and User Space: Bytes 128 ~ 255

Bytes 128 ~ 145: Module Part Number

The manufacturer's part number is written in ASCII format within these bytes. Unused digits are coded as ASCII blanks (0x20).

Bytes 146 ~ 147: Module Revision Code

This refers to the module revision code. While the SPD spec will not attempt to define the format for this information, the individual manufacturer may keep track of the revision code and its appropriate decode represented in this byte.

Byte 148: DRAM Manufacturer ID Code, Least Significant Byte**Byte 149: DRAM Manufacturer ID Code, Most Significant Byte**

This two-byte field indicates the manufacturer of the DRAM on the module, encoded as follows: the first byte is the number of continuation bytes indicated in JEP-106; the second byte is the last non-zero byte of the manufacturer's ID code, again as indicated in JEP-106.

| Byte 149, Bits 7 ~ 0 | Byte 148, Bit 7 | Byte 148, Bits 6 ~ 0 |
|--|-------------------------------------|--|
| Last non-zero byte, DRAM Manufacturer | Odd Parity for Byte 148, bits 6 ~ 0 | Number of continuation codes, DRAM Manufacturer |
| See JEP-106 | | See JEP-106 |

Examples: See examples for bytes 117~118 in SPD General Section.

Bytes 150 ~ 175: Manufacturer's Specific Data

The module manufacturer may include any additional information desired into the module within these locations.

Bytes 176 ~ 255: Open for Customer Use

These bytes are unused by the manufacturer and are open for customer use.

ASCII Decode Matrix for SPDs

The following table is a subset of the full ASCII standard which is used for coding bytes in the Serial Presence Detect EEPROM that require ASCII characters:

| First Hex Digit in Pair | Second Hex Digit in Pair | | | | | | | | | | | | | | | |
|-------------------------|--------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| 2 | Blank Space | | | | | | | (|) | | | | - | . | | |
| 3 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | | | | | | |
| 4 | | A | B | C | D | E | F | G | H | I | J | K | L | M | N | O |
| 5 | P | Q | R | S | T | U | V | W | X | Y | Z | | | | | |
| 6 | | a | b | c | d | e | f | g | h | i | j | k | l | m | n | o |
| 7 | p | q | r | s | t | u | v | w | x | y | z | | | | | |

Examples:

- 0x20 = Blank Space
- 0x34 = '4'
- 0x41 = 'A'

| SPD Bytes 128 ~ 145 | |
|---------------------|--------------------------------------|
| Manufacturer's PN | Coded in ASCII |
| 13M32734BCD-260Y | 31334D33323733344243442D323630592020 |

Annex K.1: Module Specific Bytes for Unbuffered Memory Module Types (Bytes 60 ~ 116)

This section defines the encoding of SPD bytes 60 ~ 116 when Memory Technology Key Byte 2 contains the value 0x0B and Module Type Key Byte 3 contains any of the following:

- 0x02, UDIMM
- 0x03, SO-DIMM
- 0x04, Micro-DIMM
- 0x06, Mini-UDIMM
- 0x08, 72b-SO-UDIMM
- 0x0C, 16b-SO-DIMM
- 0x0D, 32b-SO-DIMM

The following is the SPD address map for the module specific section, bytes 60 ~ 116, of the SPD for Unbuffered Module Types.

| Module Specific SPD Bytes for Unbuffered Module Types | | |
|---|---|-------|
| Byte Number | Function Described | Notes |
| 60 | Raw Card Extension, Module Nominal Height | |
| 61 | Module Maximum Thickness | |
| 62 | Reference Raw Card Used | |
| 63 | Address Mapping from Edge Connector to DRAM | |
| 64 ~ 116 | Reserved | |

Byte 60 (Unbuffered): Raw Card Extension, Module Nominal Height

The upper 3 bits of this byte define extensions to the Raw Card Revision in Byte 62. The lower 5 bits of this byte define the nominal height (A dimension) in millimeters of the fully assembled module including heat spreaders or other added components. Refer to the relevant JEDEC JC-11 module outline (MO) documents for dimension definitions.

| Bits 7 ~ 5 | Bits 4 ~ 0 |
|--|---|
| Raw Card Extension | Module Nominal Height max, in mm (baseline height = 15 mm) |
| 000 = raw card revisions 0 to 3; see byte 62 001 = raw card revision 4 010 = raw card revision 5 011 = raw card revision 6 100 = raw card revision 7 101 = raw card revision 8 110 = raw card revision 9 111 = raw card revision 10 | 00000 = height ≤ 15 mm 00001 = 15 < height ≤ 16 mm 00010 = 16 < height ≤ 17 mm 00011 = 17 < height ≤ 18 mm 00100 = 18 < height ≤ 19 mm ... 01010 = 24 < height ≤ 25 mm 01011 = 25 < height ≤ 26 mm ... 01111 = 29 < height ≤ 30 mm 10000 = 30 < height ≤ 31 mm ... 11111 = 45 mm < height |

Byte 61 (Unbuffered): Module Maximum Thickness

This byte defines the maximum thickness (E dimension) in millimeters of the fully assembled module including heat spreaders or other added components above the module circuit board surface. Thickness of the front of the module is calculated as the E1 dimension minus the PCB thickness. Thickness of the back of the module is calculated as the E dimension minus the E1 dimension. Refer to the relevant JEDEC JC-11 module outline (MO) documents for dimension definitions.

| Bits 7 ~ 4 | Bits 3 ~ 0 |
|---|---|
| Module Maximum Thickness max, Back, in mm (baseline thickness = 1 mm) | Module Maximum Thickness max, Front, in mm (baseline thickness = 1 mm) |
| 0000 = thickness ≤ 1 mm 0001 = 1 < thickness ≤ 2 mm 0010 = 2 < thickness ≤ 3 mm 0011 = 3 < thickness ≤ 4 mm ... 1110 = 14 < thickness ≤ 15 mm 1111 = 15 < thickness | 0000 = thickness ≤ 1 mm 0001 = 1 < thickness ≤ 2 mm 0010 = 2 < thickness ≤ 3 mm 0011 = 3 < thickness ≤ 4 mm ... 1110 = 14 < thickness ≤ 15 mm 1111 = 15 < thickness |
| Note Thickness = E - E1 | Note Thickness = E1 - PCB |

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Byte 62 (Unbuffered): Reference Raw Card Used

This byte indicates which JEDEC reference design raw card was used as the basis for the module assembly, if any. Bits 4 ~ 0 describe the raw card and bits 6 ~ 5 describe the revision level of that raw card. Special reference raw card indicator, ZZ, is used when no JEDEC standard raw card reference design was used as the basis for the module design. Pre-production modules should be encoded as revision 0 in bits 6 ~ 5.

| Bit 7 | Bits 6 ~ 5 | Bits 4 ~ 0 |
|--------------------------------------|---|--|
| Reference Raw Card Extension | Reference Raw Card Revision | Reference Raw Card |
| 0 = Reference raw cards A through AL | 00 = revision 0 01 = revision 1 10 = revision 2 11 = revision 3 See byte 60 for extensions beyond revision 3; for legacy systems, these bits represent the compatibility of later revisions | When bit 7 = 0, 00000 = Reference raw card A 00001 = Reference raw card B 00010 = Reference raw card C 00011 = Reference raw card D 00100 = Reference raw card E 00101 = Reference raw card F 00110 = Reference raw card G 00111 = Reference raw card H 01000 = Reference raw card J 01001 = Reference raw card K 01010 = Reference raw card L 01011 = Reference raw card M 01100 = Reference raw card N 01101 = Reference raw card P 01110 = Reference raw card R 01111 = Reference raw card T 10000 = Reference raw card U 10001 = Reference raw card V 10010 = Reference raw card W 10011 = Reference raw card Y 10100 = Reference raw card AA 10101 = Reference raw card AB 10110 = Reference raw card AC 10111 = Reference raw card AD 11000 = Reference raw card AE 11001 = Reference raw card AF 11010 = Reference raw card AG 11011 = Reference raw card AH 11100 = Reference raw card AJ 11101 = Reference raw card AK 11110 = Reference raw card AL 11111 = ZZ (no JEDEC reference raw card design used) |

| Bit 7 | Bits 6 ~ 5 | Bits 4 ~ 0 |
|---------------------------------------|---|--|
| Reference Raw Card Extension | Reference Raw Card Revision | Reference Raw Card |
| 1 = Reference raw cards AM through CB | 00 = revision 0 01 = revision 1 10 = revision 2 11 = revision 3 See byte 60 for extensions beyond revision 3; for legacy systems, these bits represent the compatibility of later revisions | When bit 7 = 1, 00000 = Reference raw card AM 00001 = Reference raw card AN 00010 = Reference raw card AP 00011 = Reference raw card AR 00100 = Reference raw card AT 00101 = Reference raw card AU 00110 = Reference raw card AV 00111 = Reference raw card AW 01000 = Reference raw card AY 01001 = Reference raw card BA 01010 = Reference raw card BB 01011 = Reference raw card BC 01100 = Reference raw card BD 01101 = Reference raw card BE 01110 = Reference raw card BF 01111 = Reference raw card BG 10000 = Reference raw card BH 10001 = Reference raw card BJ 10010 = Reference raw card BK 10011 = Reference raw card BL 10100 = Reference raw card BM 10101 = Reference raw card BN 10110 = Reference raw card BP 10111 = Reference raw card BR 11000 = Reference raw card BT 11001 = Reference raw card BU 11010 = Reference raw card BV 11011 = Reference raw card BW 11100 = Reference raw card BY 11101 = Reference raw card CA 11110 = Reference raw card CB 11111 = ZZ (no JEDEC reference raw card design used) |

Byte 63: Address Mapping from Edge Connector to DRAM

This byte describes the connection of edge connector pins for address bits to the corresponding input pins of the DDR3 SDRAMs for rank 1 only; rank 0 is always assumed to use standard mapping. Only two connection types are supported, standard or mirrored, as described in the mapping table below. System software must compensate for this mapping when issuing mode register set commands to the ranks of DDR3 SDRAMs on this module.

| Bits 7 ~ 1 | Bit 0 |
|------------|------------------------------|
| Reserved | Rank 1 Mapping |
| Reserved | 0 = standard 1 = mirrored |

The definition of standard and mirrored address connection mapping is detailed below; highlighted rows in the table indicate which signals change between mappings.

| Edge Connector Signal | DRAM Pin, Standard | DRAM Pin, Mirrored |
|-----------------------|--------------------|--------------------|
| A0 | A0 | A0 |

| Edge Connector Signal | DRAM Pin, Standard | DRAM Pin, Mirrored |
|-----------------------|----------------------|----------------------|
| A1 | A1 | A1 |
| A2 | A2 | A2 |
| A3 | A3 | A4 |
| A4 | A4 | A3 |
| A5 | A5 | A6 |
| A6 | A6 | A5 |
| A7 | A7 | A8 |
| A8 | A8 | A7 |
| A9 | A9 | A9 |
| A10/AP | A10/AP | A10/AP |
| A11 | A11 | A11 |
| A12/ \overline{BC} | A12/ \overline{BC} | A12/ \overline{BC} |
| A13 | A13 | A13 |
| A14 | A14 | A14 |
| A15/BA3 | A15/BA3 | A15/BA3 |
| BA0 | BA0 | BA1 |
| BA1 | BA1 | BA0 |
| BA2 | BA2 | BA2 |

Bytes 64 ~ 116 (Unbuffered): Reserved

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Annex K.2: Module Specific Bytes for Registered Memory Module Types (Bytes 60 ~ 116)

This section defines the encoding of SPD bytes 60 ~ 116 when Memory Technology Key Byte 2 contains the value 0x0B and Module Type Key Byte 3 contains any of the following:

- 0x01, RDIMM
- 0x05, Mini-RDIMM
- 0x09, 72b-SO-RDIMM

The following is the SPD address map for the module specific section, bytes 60 ~ 116, of the SPD for Registered Module Types.

| Module Specific SPD Bytes for Registered Module Types | | |
|---|---|-------|
| Byte Number | Function Described | Notes |
| 60 | Raw Card Extension, Module Nominal Height | |
| 61 | Module Maximum Thickness | |
| 62 | Reference Raw Card Used | |
| 63 | DIMM Module Attributes | |
| 64 | RDIMM Thermal Heat Spreader Solution | |
| 65 | Register Manufacturer ID Code, Least Significant Byte | |
| 66 | Register Manufacturer ID Code, Most Significant Byte | |
| 67 | Register Revision Number | |
| 68 | Register Type | |
| 69 | RC1 (MS Nibble) / RC0 (LS Nibble) | |
| 70 | RC3 (MS Nibble) / RC2 (LS Nibble) - Drive Strength, Command/Address | |
| 71 | RC5 (MS Nibble) / RC4 (LS Nibble) - Drive Strength, Control and Clock | |
| 72 | RC7 (MS Nibble) / RC6 (LS Nibble) | |
| 73 | RC9 (MS Nibble) / RC8 (LS Nibble) | |
| 74 | RC11 (MS Nibble) / RC10 (LS Nibble) | |
| 75 | RC13 (MS Nibble) / RC12 (LS Nibble) | |
| 76 | RC15 (MS Nibble) / RC14 (LS Nibble) | |
| 77 ~ 116 | Reserved | |

Byte 60 (Registered): Raw Card Extension, Module Nominal Height

The upper 3 bits of this byte define extensions to the Raw Card Revision in Byte 62. The lower 5 bits of this byte define the nominal height (A dimension) in millimeters of the fully assembled module including heat spreaders or other added components. Refer to the relevant JEDEC JC-11 module outline (MO) documents for dimension definitions.

| Bits 7 ~ 5 | Bits 4 ~ 0 |
|--|---|
| Raw Card Extension | Module Nominal Height max, in mm (baseline height = 15 mm) |
| 000 = raw card revisions 0 to 3; see byte 62 001 = raw card revision 4 010 = raw card revision 5 011 = raw card revision 6 100 = raw card revision 7 101 = raw card revision 8 110 = raw card revision 9 111 = raw card revision 10 | 00000 = height ≤ 15 mm 00001 = 15 < height ≤ 16 mm 00010 = 16 < height ≤ 17 mm 00011 = 17 < height ≤ 18 mm 00100 = 18 < height ≤ 19 mm ... 01010 = 24 < height ≤ 25 mm 01011 = 25 < height ≤ 26 mm ... 01111 = 29 < height ≤ 30 mm 10000 = 30 < height ≤ 31 mm ... 11111 = 45 mm < height |

Byte 61 (Registered): Module Maximum Thickness

This byte defines the maximum thickness (E dimension) in millimeters of the fully assembled module including heat spreaders or other added components above the module circuit board surface. Thickness of the front of the module is calculated as the E1 dimension minus the PCB thickness. Thickness of the back of the module is calculated as the E dimension minus the E1 dimension. Refer to the relevant JEDEC JC-11 module outline (MO) documents for dimension definitions.

| Bits 7 ~ 4 | Bits 3 ~ 0 |
|---|---|
| Module Maximum Thickness max, Back, in mm (baseline thickness = 1 mm) | Module Maximum Thickness max, Front, in mm (baseline thickness = 1 mm) |
| 0000 = thickness ≤ 1 mm 0001 = 1 < thickness ≤ 2 mm 0010 = 2 < thickness ≤ 3 mm 0011 = 3 < thickness ≤ 4 mm ... 1110 = 14 < thickness ≤ 15 mm 1111 = 15 < thickness | 0000 = thickness ≤ 1 mm 0001 = 1 < thickness ≤ 2 mm 0010 = 2 < thickness ≤ 3 mm 0011 = 3 < thickness ≤ 4 mm ... 1110 = 14 < thickness ≤ 15 mm 1111 = 15 < thickness |
| Note Thickness = E - E1 | Note Thickness = E1 - PCB |

Byte 62 (Registered): Reference Raw Card Used

This byte indicates which JEDEC reference design raw card was used as the basis for the module assembly, if any. Bits 4~0 describe the raw card and bits 6~5 describe the revision level of that raw card. Special raw card indicator, ZZ, is used when no JEDEC standard raw card was used as the basis for the design. Pre-production modules should be encoded as revision 0 in bits 6~5.

| Bit 7 | Bits 6 ~ 5 | Bits 4 ~ 0 |
|--------------------------------------|---|--|
| Reference Raw Card Extension | Reference Raw Card Revision | Reference Raw Card |
| 0 = Reference raw cards A through AL | 00 = revision 0 01 = revision 1 10 = revision 2 11 = revision 3 See byte 60 for extensions beyond revision 3; for legacy systems, these bits represent the compatibility of later revisions | When bit 7 = 0, 00000 = Reference raw card A 00001 = Reference raw card B 00010 = Reference raw card C 00011 = Reference raw card D 00100 = Reference raw card E 00101 = Reference raw card F 00110 = Reference raw card G 00111 = Reference raw card H 01000 = Reference raw card J 01001 = Reference raw card K 01010 = Reference raw card L 01011 = Reference raw card M 01100 = Reference raw card N 01101 = Reference raw card P 01110 = Reference raw card R 01111 = Reference raw card T 10000 = Reference raw card U 10001 = Reference raw card V 10010 = Reference raw card W 10011 = Reference raw card Y 10100 = Reference raw card AA 10101 = Reference raw card AB 10110 = Reference raw card AC 10111 = Reference raw card AD 11000 = Reference raw card AE 11001 = Reference raw card AF 11010 = Reference raw card AG 11011 = Reference raw card AH 11100 = Reference raw card AJ 11101 = Reference raw card AK 11110 = Reference raw card AL 11111 = ZZ (no JEDEC reference raw card design used) |

| Bit 7 | Bits 6 ~ 5 | Bits 4 ~ 0 |
|---------------------------------------|--|--|
| Reference Raw Card Extension | Reference Raw Card Revision | Reference Raw Card |
| 1 = Reference raw cards AM through CB | 00 = revision 0 01 = revision 1 10 = revision 2 11 = revision 3 or higher See byte 60 for extensions beyond revision 3 | When bit 7 = 1, 00000 = Reference raw card AM 00001 = Reference raw card AN 00010 = Reference raw card AP 00011 = Reference raw card AR 00100 = Reference raw card AT 00101 = Reference raw card AU 00110 = Reference raw card AV 00111 = Reference raw card AW 01000 = Reference raw card AY 01001 = Reference raw card BA 01010 = Reference raw card BB 01011 = Reference raw card BC 01100 = Reference raw card BD 01101 = Reference raw card BE 01110 = Reference raw card BF 01111 = Reference raw card BG 10000 = Reference raw card BH 10001 = Reference raw card BJ 10010 = Reference raw card BK 10011 = Reference raw card BL 10100 = Reference raw card BM 10101 = Reference raw card BN 10110 = Reference raw card BP 10111 = Reference raw card BR 11000 = Reference raw card BT 11001 = Reference raw card BU 11010 = Reference raw card BV 11011 = Reference raw card BW 11100 = Reference raw card BY 11101 = Reference raw card CA 11110 = Reference raw card CB 11111 = ZZ (no JEDEC reference raw card design used) |

Byte 63 (Registered): DIMM Module Attributes

This byte indicates number of registers used on a module. Further it indicates number of rows of DRAM packages (monolithic or DDP or stacked) parallel to edge connector (independent of DRAM orientation) on each side of the printed circuit board.

| Bit 7 ~ Bit 4 | Bit 3 ~ Bit 2 | Bit 1 ~ Bit 0 |
|---------------|--|---|
| Reserved | # of rows of DRAMs on RDIMM | # of Registers used on RDIMM |
| Reserved | 00 = undefined 01 = 1 row 10 = 2 rows 11 = 4 rows | 00 = Undefined 01 = 1 register 10 = 2 registers 11 = 4 registers |

Examples: DDR3 RDIMM R/C E programs byte 63 as 0x09. DDR3 RDIMM R/C F programs byte 63 as 0x0A.

Byte 64: RDIMM Thermal Heat Spreader Solution

This byte describes the module's supported thermal heat spreader solution.

| Bit 7 | Bits 6 ~ 0 |
|--|---|
| Heat Spreader Solution | Heat Spreader Thermal Characteristics |
| 0 = Heat spreader solution is not incorporated onto this assembly 1 = Heat spreader solution is incorporated onto this assembly | 0 = Undefined All other settings to be defined |

Byte 65: Register Manufacturer ID Code, Least Significant Byte

Byte 66: Register Manufacturer ID Code, Most Significant Byte

This two-byte field indicates the manufacturer of the register used on the module, encoded as follows: the first byte is the number of continuation bytes indicated in JEP-106; the second byte is the last non-zero byte of the manufacturer's ID code, again as indicated in JEP-106. These bytes are optional. For modules without the Register Manufacturer ID Code information both bytes should be programmed to 0x00.

| Byte 66, Bits 7 ~ 0 | Byte 65, Bit 7 | Byte 65 Bits 6 ~ 0 |
|--|---|--|
| Last non-zero byte, Register Manufacturer | Odd parity for Byte 65, bits 6 ~ 0 | Number of continuation codes, Register Manufacturer |
| See JEP-106 | | See JEP-106 |

Example: For "7F 7F 7F 7F 7F 51" in JEP-106.

Byte 65[6:0]: 5 continuation codes expressed in binary => 0000101

Byte 65[7]: Odd parity for byte 65[6:0] => 1

Byte 66[7:0]: Last non-zero byte from JEP-106 => 0x51

This yields 0x51 and 0x85 for bytes 66 and 65, respectively.

Also: See examples for bytes 117~118 in SPD General Section.

Byte 67: Register Revision Number

This byte defines the vendor die revision level of the registering clock driver component. This byte is optional. For modules without the Register Revision Number information, this byte should be programmed to 0xFF.

| Bits 7 ~ 0 |
|---|
| Register Revision Number |
| Programmed in straight Hex format - no conversion needed. |
| 00 - Valid |
| 01 - Valid |
| .. |
| FE - Valid |
| FF - Undefined (No Rev Number Provided) |

Examples:

| Code | Meaning |
|------|--------------|
| 0x00 | Revision 0 |
| 0x01 | Revision 1 |
| 0x31 | Revision 3.1 |
| 0xA3 | Revision A3 |
| 0xB1 | Revision B1 |

Byte 68 Register Type

This byte defines the type of support device that is used on this RDIMM assembly. It is used as an index for SPD Bytes 69 ~ 76 to determine the interpretation of personality word programming and other register or DIMM implementation specific features.

| Bits 7 ~ 3 | Bit 2 | Bit 1 | Bit 0 | Support Device |
|------------|---------------------|-------|-------|----------------|
| Reserved | 0 | 0 | 0 | SSTE32882 |
| | All other encodings | | | Reserved |

The programming of SPD bytes 69 ~ 76 is related to multiple documents including the DDR3 Registered DIMM Specification, the SSTE32882 Registering Clock Driver specification, register supplier data sheets, and DIMM supplier data sheets.

For JEDEC standard raw cards, the programming of the register control words is described in the DDR3 Registered DIMM Specification (in the appendices for each raw card), and the programming of the SPD bytes corresponding to the register control words is described in Bytes 69 ~ 76 below. Where control words or control bits are defined as RFU in the SPD specification, the SPD bytes and bits must be set to 0 to ensure future compatibility.

Custom registered DIMM designs should use the JEDEC standard designs as guidelines as much as possible, then refer to the JEDEC SSTE32882 specification and register supplier data sheets for detailed information on programming the devices. Simulation and testing are recommended to ensure proper operation in target systems. Where control words or control bits are defined as RFU in the SPD specification, users should refer to these other documents for programming details. The SPD bytes and bits must be set to 0 to ensure future compatibility, however these values may or may not be the required values sent to the register for proper operation. System BIOS writers in particular should make themselves aware of the effects of each register programming code.

Byte 69 [SSTE32882]: RC1 (MS Nibble) / RC0 (LS Nibble) - Reserved

This byte is currently reserved for future use.

| RC1 - Reserved, RC0 - Reserved | | | | | | | |
|--|------------|-----------|-----------|------------|------------|-----------|-----------|
| RC1 | | | | RC0 | | | |
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| DBA1 value | DBA0 value | DA4 value | DA3 value | DBA1 value | DBA0 value | DA4 value | DA3 value |
| Note 1 Reserved for future use. SPD must be programmed as 0x00; refer to the RDIMM and register specifications for programming details. | | | | | | | |

Byte 70 [SSTE32882]: RC3 (MS Nibble) / RC2 (LS Nibble) - Drive Strength, Command/Address.

This byte defines the drive strength for addresses, commands (RC3) appropriate for the RDIMM design. LS Nibble is RESERVED for future use. This byte is referenced directly from the SSTE32882 specification.

| RC2 - Timing Control Word, RC3 - Drive Strength: Command/Address | | | | | | | |
|---|------------|---|-----------|---|------------|-----------|-----------|
| RC3 | | | | RC2 | | | |
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| DBA1 value | DBA0 value | DA4 value | DA3 value | DBA1 value | DBA0 value | DA4 value | DA3 value |
| Command/Address, B Outputs | | Command/Address, A Outputs | | Notes: Reserved for future use. SPD must be programmed as 0000. Refer to the RDIMM and register specifications for programming details. | | | |
| 00 = Light Drive 01 = Moderate Drive 10 = Strong Drive 11 = Reserved | | 00 = Light Drive 01 = Moderate Drive 10 = Strong Drive 11 = Reserved | | | | | |
| Note 1 Standard values for RC3 are defined in the DDR3 Registered DIMM Reference Design Specification for JEDEC standard module reference designs. | | | | | | | |

Byte 71 [SSTE32882]: RC5 (MS Nibble) / RC4 (LS Nibble) - Drive Strength, Control and Clock

The control word location for the driver strength for control signals for the SSTE32882 is RC4. The control word location for the clock driver strength for the SSTE32882 is RC5. This byte defines the drive strength for clocks appropriate for the RDIMM design. This byte is referenced directly from the SSTE32882 specification.

| RC5 - Drive Strength Clock, RC4 - Drive Strength: Control | | | | | | | |
|---|------------|---|-----------|---|------------|---|-----------|
| RC5 | | | | RC4 | | | |
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| DBA1 value | DBA0 value | DA4 value | DA3 value | DBA1 value | DBA0 value | DA4 value | DA3 value |
| Y0/Y0# and Y2/Y2# Clock Outputs | | Y1/Y1# and Y3/Y3# Clock Outputs | | Control Signals, B Outputs | | Control Signals, A Outputs | |
| 00 = Light Drive 01 = Moderate Drive 10 = Strong Drive 11 = Reserved | | 00 = Light Drive 01 = Moderate Drive 10 = Strong Drive 11 = Reserved | | 00 = Light Drive 01 = Moderate Drive 10 = Reserved 11 = Reserved | | 00 = Light Drive 01 = Moderate Drive 10 = Reserved 11 = Reserved | |
| Note 1 Standard values for RC5 and RC4 are defined in the DDR3 Registered DIMM Reference Design Specification for JEDEC standard module reference designs. | | | | | | | |

Byte 72 [SSTE32882]: RC7 (MS Nibble) / RC6 (LS Nibble) - Reserved for Register Vendor Specific Modes

Register control words RC7 & RC6 are reserved for register vendor specific purposes (for example, register test modes). The corresponding SPD byte 72 should be programmed to 0x00 for normal operation.

| RC7 - Register Vendor Defined, RC6 - Register Vendor Defined | | | | | | | |
|--|------------|-----------|-----------|------------|------------|-----------|-----------|
| RC7 | | | | RC6 | | | |
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| DBA1 value | DBA0 value | DA4 value | DA3 value | DBA1 value | DBA0 value | DA4 value | DA3 value |
| Note 1 Reserved for future use. SPD must be programmed as 0x00; refer to the RDIMM and register specifications for programming details. | | | | | | | |

Byte 73 [SSTE32882]: RC9 (MS Nibble) / RC8 (LS Nibble) - Reserved

This byte is currently reserved for future use.

| RC9 - Reserved, RC8 - Reserved | | | | | | | |
|--|------------|-----------|-----------|------------|------------|-----------|-----------|
| RC9 | | | | RC8 | | | |
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| DBA1 value | DBA0 value | DA4 value | DA3 value | DBA1 value | DBA0 value | DA4 value | DA3 value |
| Note 1 Reserved for future use. SPD must be programmed as 0x00; refer to the RDIMM and register specifications for programming details. | | | | | | | |

Byte 74 [SSTE32882]: RC11 (MS Nibble) / RC10 (LS Nibble) - Reserved

This byte is currently reserved for future use.

| RC11 - Reserved, RC10 - Reserved | | | | | | | |
|--|------------|-----------|-----------|------------|------------|-----------|-----------|
| RC11 | | | | RC10 | | | |
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| DBA1 value | DBA0 value | DA4 value | DA3 value | DBA1 value | DBA0 value | DA4 value | DA3 value |
| Note 1 Reserved for future use. SPD must be programmed as 0x00; refer to the RDIMM and register specifications for programming details. | | | | | | | |

Byte 75 [SSTE32882]: RC13 (MS Nibble) / RC12 (LS Nibble) - Reserved

This byte is currently reserved for future use.

| RC13 - Reserved, RC12 - Reserved | | | | | | | |
|--|------------|-----------|-----------|------------|------------|-----------|-----------|
| RC13 | | | | RC12 | | | |
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| DBA1 value | DBA0 value | DA4 value | DA3 value | DBA1 value | DBA0 value | DA4 value | DA3 value |
| Note 1 Reserved for future use. SPD must be programmed as 0x00; refer to the RDIMM and register specifications for programming details. | | | | | | | |

Byte 76 [SSTE32882]: RC15 (MS Nibble) / RC14 (LS Nibble) - Reserved

This byte is currently reserved for future use.

| RC15 - Reserved, RC14 - Reserved | | | | | | | |
|--|------------|-----------|-----------|------------|------------|-----------|-----------|
| RC15 | | | | RC14 | | | |
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| DBA1 value | DBA0 value | DA4 value | DA3 value | DBA1 value | DBA0 value | DA4 value | DA3 value |
| Note 1 Reserved for future use. SPD must be programmed as 0x00; refer to the RDIMM and register specifications for programming details. | | | | | | | |

Bytes 77 ~ 116 (Registered): Reserved

Annex K.3: Module Specific Bytes for Clocked Memory Module Types (Bytes 60 ~ 116)

This section defines the encoding of SPD bytes 60 ~ 116 when Memory Technology Key Byte 2 contains the value 0x0B and Module Type Key Byte 3 contains any of the following:

- 0x07, Mini-CDIMM
- 0x0A, 72b-SO-CDIMM

The following is the SPD address map for the module specific section, bytes 60 ~ 116, of the SPD for Unbuffered Module Types.

| Module Specific SPD Bytes for Unbuffered Module Types | | |
|---|---|-------|
| Byte Number | Function Described | Notes |
| 60 | Raw Card Extension, Module Nominal Height | |
| 61 | Module Maximum Thickness | |
| 62 | Reference Raw Card Used | |
| 63 ~ 116 | Reserved | |

Byte 60 (Clocked): Raw Card Extension, Module Nominal Height

The upper 3 bits of this byte define extensions to the Raw Card Revision in Byte 62. The lower 5 bits of this byte define the nominal height (A dimension) in millimeters of the fully assembled module including heat spreaders or other added components. Refer to the relevant JEDEC JC-11 module outline (MO) documents for dimension definitions.

| Bits 7 ~ 5 | Bits 4 ~ 0 |
|--|---|
| Raw Card Extension | Module Nominal Height max, in mm (baseline height = 15 mm) |
| 000 = raw card revisions 0 to 3; see byte 62 | 00000 = height ≤ 15 mm |
| 001 = raw card revision 4 | 00001 = 15 < height ≤ 16 mm |
| 010 = raw card revision 5 | 00010 = 16 < height ≤ 17 mm |
| 011 = raw card revision 6 | 00011 = 17 < height ≤ 18 mm |
| 100 = raw card revision 7 | 00100 = 18 < height ≤ 19 mm |
| 101 = raw card revision 8 | ... |
| 110 = raw card revision 9 | 01010 = 24 < height ≤ 25 mm |
| 111 = raw card revision 10 | 01011 = 25 < height ≤ 26 mm |
| | ... |
| | 01111 = 29 < height ≤ 30 mm |
| | 10000 = 30 < height ≤ 31 mm |
| | ... |
| | 11111 = 45 mm < height |

Byte 61 (Clocked): Module Maximum Thickness

This byte defines the maximum thickness (E dimension) in millimeters of the fully assembled module including heat spreaders or other added components above the module circuit board surface. Thickness of the front of the module is calculated as the E1 dimension minus the PCB thickness. Thickness of the back of the module is calculated as the E dimension minus the E1 dimension. Refer to the relevant JEDEC JC-11 module outline (MO) documents for dimension definitions.

| Bits 7 ~ 4 | Bits 3 ~ 0 |
|---|---|
| Module Maximum Thickness max, Back, in mm (baseline thickness = 1 mm) | Module Maximum Thickness max, Front, in mm (baseline thickness = 1 mm) |
| 0000 = thickness ≤ 1 mm 0001 = 1 < thickness ≤ 2 mm 0010 = 2 < thickness ≤ 3 mm 0011 = 3 < thickness ≤ 4 mm ... 1110 = 14 < thickness ≤ 15 mm 1111 = 15 < thickness | 0000 = thickness ≤ 1 mm 0001 = 1 < thickness ≤ 2 mm 0010 = 2 < thickness ≤ 3 mm 0011 = 3 < thickness ≤ 4 mm ... 1110 = 14 < thickness ≤ 15 mm 1111 = 15 < thickness |
| Note Thickness = E - E1 | Note Thickness = E1 - PCB |

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Byte 62 (Clocked): Reference Raw Card Used

This byte indicates which JEDEC reference design raw card was used as the basis for the module assembly, if any. Bits 4 ~ 0 describe the raw card and bits 6 ~ 5 describe the revision level of that raw card. Special reference raw card indicator, ZZ, is used when no JEDEC standard raw card reference design was used as the basis for the module design. Pre-production modules should be encoded as revision 0 in bits 6 ~ 5.

| Bit 7 | Bits 6 ~ 5 | Bits 4 ~ 0 |
|--------------------------------------|---|--|
| Reference Raw Card Extension | Reference Raw Card Revision | Reference Raw Card |
| 0 = Reference raw cards A through AL | 00 = revision 0 01 = revision 1 10 = revision 2 11 = revision 3 See byte 60 for extensions beyond revision 3; for legacy systems, these bits represent the compatibility of later revisions | When bit 7 = 0, 00000 = Reference raw card A 00001 = Reference raw card B 00010 = Reference raw card C 00011 = Reference raw card D 00100 = Reference raw card E 00101 = Reference raw card F 00110 = Reference raw card G 00111 = Reference raw card H 01000 = Reference raw card J 01001 = Reference raw card K 01010 = Reference raw card L 01011 = Reference raw card M 01100 = Reference raw card N 01101 = Reference raw card P 01110 = Reference raw card R 01111 = Reference raw card T 10000 = Reference raw card U 10001 = Reference raw card V 10010 = Reference raw card W 10011 = Reference raw card Y 10100 = Reference raw card AA 10101 = Reference raw card AB 10110 = Reference raw card AC 10111 = Reference raw card AD 11000 = Reference raw card AE 11001 = Reference raw card AF 11010 = Reference raw card AG 11011 = Reference raw card AH 11100 = Reference raw card AJ 11101 = Reference raw card AK 11110 = Reference raw card AL 11111 = ZZ (no JEDEC reference raw card design used) |

| Bit 7 | Bits 6 ~ 5 | Bits 4 ~ 0 |
|---------------------------------------|---|--|
| Reference Raw Card Extension | Reference Raw Card Revision | Reference Raw Card |
| 1 = Reference raw cards AM through CB | 00 = revision 0 01 = revision 1 10 = revision 2 11 = revision 3 See byte 60 for extensions beyond revision 3; for legacy systems, these bits represent the compatibility of later revisions | When bit 7 = 1, 00000 = Reference raw card AM 00001 = Reference raw card AN 00010 = Reference raw card AP 00011 = Reference raw card AR 00100 = Reference raw card AT 00101 = Reference raw card AU 00110 = Reference raw card AV 00111 = Reference raw card AW 01000 = Reference raw card AY 01001 = Reference raw card BA 01010 = Reference raw card BB 01011 = Reference raw card BC 01100 = Reference raw card BD 01101 = Reference raw card BE 01110 = Reference raw card BF 01111 = Reference raw card BG 10000 = Reference raw card BH 10001 = Reference raw card BJ 10010 = Reference raw card BK 10011 = Reference raw card BL 10100 = Reference raw card BM 10101 = Reference raw card BN 10110 = Reference raw card BP 10111 = Reference raw card BR 11000 = Reference raw card BT 11001 = Reference raw card BU 11010 = Reference raw card BV 11011 = Reference raw card BW 11100 = Reference raw card BY 11101 = Reference raw card CA 11110 = Reference raw card CB 11111 = ZZ (no JEDEC reference raw card design used) |

Bytes 63 ~ 116 (Clocked): Reserved

Annex K.4: Module Specific Bytes for Load Reduced Memory Module Types (Bytes 60 ~ 116)

This section defines the encoding of SPD bytes 60 ~ 116 when Memory Technology Key Byte 2 contains the value 0x0B and Module Type Key Byte 3 contains any of the following:

- 0x0B, LRDIMM

The following is the SPD address map for the module specific section, bytes 60 ~ 116, of the SPD for Load Reduced Module Types.

| Module Specific SPD Bytes for Load Reduced Module Types | | |
|---|--|-------|
| Byte Number | Function Described | Notes |
| 60 | Raw Card Extension, Module Nominal Height | |
| 61 | Module Maximum Thickness | |
| 62 | Reference Raw Card Used | |
| 63 | Module Attributes | |
| 64 | Memory Buffer Revision ID | |
| 65 | Memory Buffer Manufacturer ID Code, Least Significant Byte | |
| 66 | Memory Buffer Manufacturer ID Code, Most Significant Byte | |
| 67 | F0RC3 / F0RC2 - Timing Control & Drive Strength, CA & CS | |
| 68 | F0RC5 / F0RC4 - Drive Strength, ODT & CKE and Y | |
| 69 | F1RC11 / F1RC8 - Extended Delay for Y, CS and ODT & CKE | |
| 70 | F1RC13 / F1RC12 - Additive Delay for CS and CA | |
| 71 | F1RC15 / F1RC14 - Additive Delay for ODT & CKE | |
| 72 | F3RC9 / F3RC8 - MDQ Termination and Drive Strength for 800 & 1066 | |
| 73 | F[3,4]RC11 / F[3,4]RC10 - Rank 0 & 1 RD & WR QxODT Control for 800 & 1066 | |
| 74 | F[5,6]RC11 / F[5,6]RC10 - Rank 2 & 3 RD & WR QxODT Control for 800 & 1066 | |
| 75 | F[7,8]RC11 / F[7,8]RC10 - Rank 4 & 5 RD & WR QxODT Control for 800 & 1066 | |
| 76 | F[9,10]RC11 / F[9,10]RC10 - Rank 6 & 7 RD & WR QxODT Control for 800 & 1066 | |
| 77 | MR1,2 Registers for 800 & 1066 | |
| 78 | F3RC9 / F3RC8 - MDQ Termination and Drive Strength for 1333 & 1600 | |
| 79 | F[3,4]RC11 / F[3,4]RC10 - Rank 0 & 1 RD & WR QxODT Control for 1333 & 1600 | |
| 80 | F[5,6]RC11 / F[5,6]RC10 - Rank 2 & 3 RD & WR QxODT Control for 1333 & 1600 | |
| 81 | F[7,8]RC11 / F[7,8]RC10 - Rank 4 & 5 RD & WR QxODT Control for 1333 & 1600 | |
| 82 | F[9,10]RC11 / F[9,10]RC10 - Rank 6 & 7 RD & WR QxODT Control for 1333 & 1600 | |
| 83 | MR1,2 Registers for 1333 & 1600 | |
| 84 | F3RC9 / F3RC8 - MDQ Termination and Drive Strength for 1866 & 2133 | |
| 85 | F[3,4]RC11 / F[3,4]RC10 - Rank 0 & 1 RD & WR QxODT Control for 1866 & 2133 | |
| 86 | F[5,6]RC11 / F[5,6]RC10 - Rank 2 & 3 RD & WR QxODT Control for 1866 & 2133 | |
| 87 | F[7,8]RC11 / F[7,8]RC10 - Rank 4 & 5 RD & WR QxODT Control for 1866 & 2133 | |
| 88 | F[9,10]RC11 / F[9,10]RC10 - Rank 6 & 7 RD & WR QxODT Control for 1866 & 2133 | |
| 89 | MR1,2 Registers for 1866 & 2133 | |
| 90 | Minimum Module Delay Time for 1.5 V | |

| Module Specific SPD Bytes for Load Reduced Module Types | | |
|--|--------------------------------------|-------|
| Byte Number | Function Described | Notes |
| 91 | Maximum Module Delay Time for 1.5 V | |
| 92 | Minimum Module Delay Time for 1.35 V | |
| 93 | Maximum Module Delay Time for 1.35 V | |
| 94 | Minimum Module Delay Time for 1.25 V | |
| 95 | Maximum Module Delay Time for 1.25 V | |
| 96~101 | Reserved | |
| 102~116 | Memory Buffer Personality Bytes | 1 |
| Note 1 These bytes were relocated between LRDIMM SPD revisions 0.1 and 0.5. | | |

Byte 60 (Load Reduced): Raw Card Extension, Module Nominal Height

The upper 3 bits of this byte define extensions to the Raw Card Revision in Byte 62. The lower 5 bits of this byte define the nominal height (A dimension) in millimeters of the fully assembled module including heat spreaders or other added components. Refer to the relevant JEDEC JC-11 module outline (MO) documents for dimension definitions.

| Bits 7 ~ 5 | Bits 4 ~ 0 |
|--|---|
| Raw Card Extension | Module Nominal Height max, in mm (baseline height = 15 mm) |
| 000 = raw card revisions 0 to 3; see byte 62 | 00000 = height ≤ 15 mm |
| 001 = raw card revision 4 | 00001 = 15 < height ≤ 16 mm |
| 010 = raw card revision 5 | 00010 = 16 < height ≤ 17 mm |
| 011 = raw card revision 6 | 00011 = 17 < height ≤ 18 mm |
| 100 = raw card revision 7 | 00100 = 18 < height ≤ 19 mm |
| 101 = raw card revision 8 | ... |
| 110 = raw card revision 9 | 01010 = 24 < height ≤ 25 mm |
| 111 = raw card revision 10 | 01011 = 25 < height ≤ 26 mm |
| | ... |
| | 01111 = 29 < height ≤ 30 mm |
| | 10000 = 30 < height ≤ 31 mm |
| | ... |
| | 11111 = 45 mm < height |

Byte 61 (Load Reduced): Module Maximum Thickness

This byte defines the maximum thickness (E dimension) in millimeters of the fully assembled module including heat spreaders or other added components above the module circuit board surface. Thickness of the front of the module is calculated as the E1 dimension minus the PCB thickness. Thickness of the back of the module is calculated as the E dimension minus the E1 dimension. Refer to the relevant JEDEC JC-11 module outline (MO) documents for dimension definitions.

| Bits 7 ~ 4 | Bits 3 ~ 0 |
|--|--|
| Module Maximum Thickness max, Back, in mm (baseline thickness = 1 mm) | Module Maximum Thickness max, Front, in mm (baseline thickness = 1 mm) |
| 0000 = thickness \leq 1 mm 0001 = 1 < thickness \leq 2 mm 0010 = 2 < thickness \leq 3 mm 0011 = 3 < thickness \leq 4 mm ... 1110 = 14 < thickness \leq 15 mm 1111 = 15 < thickness | 0000 = thickness \leq 1 mm 0001 = 1 < thickness \leq 2 mm 0010 = 2 < thickness \leq 3 mm 0011 = 3 < thickness \leq 4 mm ... 1110 = 14 < thickness \leq 15 mm 1111 = 15 < thickness |
| Note Thickness = E - E1 | Note Thickness = E1 - PCB |

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Byte 62 (Load Reduced): Reference Raw Card Used

This byte indicates which JEDEC reference design raw card was used as the basis for the module assembly, if any. Bits 4~0 describe the raw card and bits 6~5 describe the revision level of that raw card. Special raw card indicator, ZZ, is used when no JEDEC standard raw card was used as the basis for the design. Pre-production modules should be encoded as revision 0 in bits 6~5.

| Bit 7 | Bits 6 ~ 5 | Bits 4 ~ 0 |
|--------------------------------------|--|--|
| Reference Raw Card Extension | Reference Raw Card Revision | Reference Raw Card |
| 0 = Reference raw cards A through AL | 00 = revision 0 01 = revision 1 10 = revision 2 11 = revision 3 or higher See byte 60 for extensions beyond revision 3 | When bit 7 = 0, 00000 = Reference raw card A 00001 = Reference raw card B 00010 = Reference raw card C 00011 = Reference raw card D 00100 = Reference raw card E 00101 = Reference raw card F 00110 = Reference raw card G 00111 = Reference raw card H 01000 = Reference raw card J 01001 = Reference raw card K 01010 = Reference raw card L 01011 = Reference raw card M 01100 = Reference raw card N 01101 = Reference raw card P 01110 = Reference raw card R 01111 = Reference raw card T 10000 = Reference raw card U 10001 = Reference raw card V 10010 = Reference raw card W 10011 = Reference raw card Y 10100 = Reference raw card AA 10101 = Reference raw card AB 10110 = Reference raw card AC 10111 = Reference raw card AD 11000 = Reference raw card AE 11001 = Reference raw card AF 11010 = Reference raw card AG 11011 = Reference raw card AH 11100 = Reference raw card AJ 11101 = Reference raw card AK 11110 = Reference raw card AL 11111 = ZZ (no JEDEC reference raw card design used) |

| Bit 7 | Bits 6 ~ 5 | Bits 4 ~ 0 |
|---------------------------------------|--|--|
| Reference Raw Card Extension | Reference Raw Card Revision | Reference Raw Card |
| 1 = Reference raw cards AM through CB | 00 = revision 0 01 = revision 1 10 = revision 2 11 = revision 3 or higher See byte 60 for extensions beyond revision 3 | When bit 7 = 1, 00000 = Reference raw card AM 00001 = Reference raw card AN 00010 = Reference raw card AP 00011 = Reference raw card AR 00100 = Reference raw card AT 00101 = Reference raw card AU 00110 = Reference raw card AV 00111 = Reference raw card AW 01000 = Reference raw card AY 01001 = Reference raw card BA 01010 = Reference raw card BB 01011 = Reference raw card BC 01100 = Reference raw card BD 01101 = Reference raw card BE 01110 = Reference raw card BF 01111 = Reference raw card BG 10000 = Reference raw card BH 10001 = Reference raw card BJ 10010 = Reference raw card BK 10011 = Reference raw card BL 10100 = Reference raw card BM 10101 = Reference raw card BN 10110 = Reference raw card BP 10111 = Reference raw card BR 11000 = Reference raw card BT 11001 = Reference raw card BU 11010 = Reference raw card BV 11011 = Reference raw card BW 11100 = Reference raw card BY 11101 = Reference raw card CA 11110 = Reference raw card CB 11111 = ZZ (no JEDEC reference raw card design used) |

Byte 63 (Load Reduced): Module Attributes

This byte describes the connection of Memory Buffer pins for address bits to the corresponding input pins of the DDR3 SDRAMs. Only two connection types are currently supported, all rank non-mirrored or odd ranks mirrored, as described in the mapping table below. System software must compensate for this mapping when issuing mode register set commands to the ranks of DDR3 SDRAMs on this module.

| Bits 3 ~ 2 | Bits 1 ~ 0 |
|--|--|
| # of rows of DRAMs | Mirroring |
| 00 = undefined 01 = 1 row 10 = 2 rows 11 = Reserved | 00 = All ranks are non-mirrored 01 = Odd ranks are mirrored 10 = Reserved 11 = Reserved |

| Bit 7 | Bit 6 | Bit 5 | Bit 4 |
|--|----------|--|--|
| Heat Spreader | Reserved | Rank Numbering | Orientation of Memory Buffer |
| 0 = Heat spreader solution is not incorporated onto this assembly 1 = Heat spreader solution is incorporated onto this assembly | Reserved | 0 = Ranks are numbered contiguously starting from rank 0 (e.g. 0, 1, 2, 3 for QR DIMM) 1 = Only even ranks starting from rank 0 are present (e.g. 0, 2, 4, 6 for QR DIMM) | 0 = Vertical MB Orientation 1 = Horizontal MB Orientation |

Byte 63 bits 1~0: The definition of non-mirrored and mirrored address connection mapping is detailed below; highlighted rows in the table indicate which signals change between mappings.

| Memory Buffer Pin | DRAM Pin, Non-mirrored | DRAM Pin, Mirrored |
|-------------------|------------------------|--------------------|
| A0 | A0 | A0 |
| A1 | A1 | A1 |
| A2 | A2 | A2 |
| A3 | A3 | A4 |
| A4 | A4 | A3 |
| A5 | A5 | A6 |
| A6 | A6 | A5 |
| A7 | A7 | A8 |
| A8 | A8 | A7 |
| A9 | A9 | A9 |
| A10/AP | A10/AP | A10/AP |
| A11 | A11 | A11 |
| A12/BC_n | A12/BC_n | A12/BC_n |
| A13 | A13 | A13 |
| A14 | A14 | A14 |
| A15 | A15 | A15 |
| BA0 | BA0 | BA1 |
| BA1 | BA1 | BA0 |
| BA2 | BA2 | BA2 |

Byte 63 bit 3: Indicates number of rows of DRAM packages (monolithic, DDP, or stacked) parallel to the edge connector (independent of DRAM orientation) on each side of the printed circuit board.

Byte 63 bit 4: Indicates the orientation, vertical or horizontal, of the Memory Buffer, with respect to the edge connector.

Byte 63 bit 5: Indicates the rank numbering on the module. The purpose of this bit is for LRDIMMs where DRAMs have been removed to facilitate signal probing.

Byte 63 bit 6: Reserved; must be 0.

Byte 63 bit 7: Describes if the module assembly incorporates a heat spreader.

Examples:

| Raw Card | Byte 63 Coding | Meaning |
|----------|----------------|--|
| C | 0x89 | Heat spreader Contiguous ranks Vertical Memory Buffer 2 rows of DRAMs Odd ranks are mirrored |
| F | 0x94 | Heat spreader Contiguous ranks Horizontal Memory Buffer 1 row of DRAMs No rank mirroring |

Byte 64 (Load Reduced): Memory Buffer Revision Number

This byte defines the vendor die revision level of the memory buffer component. This byte is optional.

| Bits 7 ~ 0 |
|---|
| Register Revision Number |
| Programmed in straight Hex format - no conversion needed. 00 - Valid 01 - Valid .. FE - Valid FF - Undefined (No Revision Number Provided) |

Examples:

| Code | Meaning |
|------|--------------|
| 0x00 | Revision 0 |
| 0x01 | Revision 1 |
| 0x31 | Revision 3.1 |
| 0xA3 | Revision A3 |
| 0xB1 | Revision B1 |

Byte 65 (Load Reduced): Memory Buffer Manufacturer ID Code, Least Significant Byte

Byte 66 (Load Reduced): Memory Buffer Manufacturer ID Code, Most Significant Byte

This two-byte field indicates the manufacturer of the memory buffer used on the module, encoded as follows: the first byte is the number of continuation bytes indicated in JEP-106; the second byte is the last non-zero byte of the manufacturer's ID code, again as indicated in JEP-106. These bytes are optional.

| Byte 66, Bits 7 ~ 0 | Byte 65, Bit 7 | Byte 65 Bits 6 ~ 0 |
|--|------------------------------------|--|
| Last non-zero byte, Memory Buffer Manufacturer | Odd parity for Byte 65, bits 6 ~ 0 | Number of continuation codes, Memory Buffer Manufacturer |
| See JEP-106 | | See JEP-106 |

Example: For “7F 7F 7F 7F 7F 51” in JEP-106.
 Byte 65[6:0]: 5 continuation codes expressed in binary => 0000101
 Byte 65[7]: Odd parity for byte 65[6:0] => 1
 Byte 66[7:0]: Last non-zero byte from JEP-106 => 0x51
 This yields 0x51 and 0x85 for bytes 66 and 65, respectively.

Also: See examples for bytes 117~118 in SPD General Section.

Byte 67 (Load Reduced): F0RC3 / F0RC2 - Timing Control & Drive Strength, Address/Command & QxCS_n

This byte defines the drive strength for addresses, commands (F0RC3) appropriate for the LRDIMM design. LS Nibble is for Timing Control use. This byte is referenced directly from the Memory Buffer specification.

| F0RC3 - Drive Strength: Address/Command, F0RC2 - Timing Control | | | | | | | |
|--|------------|--|-----------|--------------------------------|------------|--------------------------------|--|
| F0RC3 | | | | F0RC2 | | | |
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| DBA1 value | DBA0 value | DA4 value | DA3 value | DBA1 value | DBA0 value | DA4 value | DA3 value |
| QxCS[3:0]_n Outputs | | Address/Command Outputs | | Reserved | Reserved | Rank 1 and Rank 5 Swap | Address/Command prelaunch |
| 00 = Light Drive 01 = Moderate Drive 10 = Strong Drive 11 = Reserved | | 00 = Light Drive 01 = Moderate Drive 10 = Strong Drive 11 = Very Strong Drive | | 0 = Operation 1 = Test Mode | | 0 = Not swapped 1 = Swapped | 0 = Standard (1/2 clock) 1 = Controlled by F1RC12 |
| Note 1 Standard values for F0RC3 and F0RC2 are defined in the DDR3 LRDIMM Reference Design Specification for JEDEC standard module reference designs. | | | | | | | |

Byte 68 (Load Reduced): F0RC5 / F0RC4 - Drive Strength, QxODT & QxCKE and Clock

The control word location for the driver strength for QxODT & QxCKE control signals for LRDIMMs is F0RC4. The control word location for the clock driver strength for LRDIMMs is F0RC5. This byte is referenced directly from the Memory Buffer specification.

| F0RC5 - Drive Strength Clock, F0RC4 - Drive Strength: QxODT & QxCKE | | | | | | | |
|---|------------|---------------------------------------|-----------|--------------------|------------|--------------------|-----------|
| F0RC5 | | | | F0RC4 | | | |
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| DBA1 value | DBA0 value | DA4 value | DA3 value | DBA1 value | DBA0 value | DA4 value | DA3 value |
| Y0_t/Y0_c and Y2_t/Y2_c Clock Outputs | | Y1_t/Y1_c and Y3_t/Y3_c Clock Outputs | | QxCKE[3:0] Outputs | | QxODT[1:0] Outputs | |

| F0RC5 - Drive Strength Clock, F0RC4 - Drive Strength: QxODT & QxCKE | | | | | | | |
|--|-------|---|-------|---|-------|---|-------|
| F0RC5 | | | | F0RC4 | | | |
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 00 = Light Drive 01 = Moderate Drive 10 = Strong Drive 11 = Reserved | | 00 = Light Drive 01 = Moderate Drive 10 = Strong Drive 11 = Reserved | | 00 = Light Drive 01 = Moderate Drive 10 = Strong Drive 11 = Reserved | | 00 = Light Drive 01 = Moderate Drive 10 = Strong Drive 11 = Reserved | |
| Note 1 Standard values for F0RC5 and F0RC4 are defined in the DDR3 LRDIMM Reference Design Specification for JEDEC standard module reference designs. | | | | | | | |

Byte 69 (Load Reduced): F1RC11 / F1RC8 - Extended Delay for Clocks, QxCS_n and QxODT & QxCKE

The control word location for the extended delay for Y clocks and QxCS_n for LRDIMMs is F1RC8. The control word location for the extended delay for QxODT & QxCKE control signals for LRDIMMs is F1RC11. This byte is referenced directly from the Memory Buffer specification.

| F1RC11 - Ext Delay for QxODT & QxCKE, F1RC8 - Ext Delay for Clocks and QxCS_n | | | | | | | |
|---|------------|--|-----------|--|------------|--|-----------|
| F1RC11 | | | | F1RC8 | | | |
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| DBA1 value | DBA0 value | DA4 value | DA3 value | DBA1 value | DBA0 value | DA4 value | DA3 value |
| QxCKE Extended Delay | | QxODT Extended Delay | | QxCS_n Extended Delay | | Y Extended Delay | |
| 00 = 0 01 = (1/128)*tCK 10 = (2/128)*tCK 11 = (3/128)*tCK | | 00 = 0 01 = (1/128)*tCK 10 = (2/128)*tCK 11 = (3/128)*tCK | | 00 = 0 01 = (1/128)*tCK 10 = (2/128)*tCK 11 = (3/128)*tCK | | 00 = 0 01 = (1/128)*tCK 10 = (2/128)*tCK 11 = (3/128)*tCK | |
| Note 1 Standard values for F1RC11 and F1RC8 are defined in the DDR3 LRDIMM Reference Design Specification for JEDEC standard module reference designs. | | | | | | | |

Byte 70 (Load Reduced): F1RC13 / F1RC12 - Additive Delay for QxCS_n and QxCA

The control word location for the additive delay for QxCA signals for LRDIMMs is F1RC12. The control word location for the additive delay for the QxCS_n control signals for LRDIMMs is F1RC13. This byte is referenced directly from the Memory Buffer specification.

| F1RC13 - Additive Delay for QxCS_n, F1RC12 - Additive Delay for Y Clocks | | | | | | | |
|--|--|-----------|-----------|------------|--|-----------|-----------|
| F1RC13 | | | | F1RC12 | | | |
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| DBA1 value | DBA0 value | DA4 value | DA3 value | DBA1 value | DBA0 value | DA4 value | DA3 value |
| QxCS_n Delay | | | | Reserved | Delay Y | | |
| 0 = Disabled 1 = Enabled | 000 = Delay QxCS_n by (8/32)*tCK 001 = Delay QxCS_n by (7/32)*tCK 010 = Delay QxCS_n by (6/32)*tCK 011 = Delay QxCS_n by (5/32)*tCK 100 = Delay QxCS_n by (4/32)*tCK 101 = Delay QxCS_n by (3/32)*tCK 110 = Delay QxCS_n by (2/32)*tCK 111 = Delay QxCS_n by (1/32)*tCK | | | | 000 = Delay Y by (8/32)*tCK 001 = Delay Y by (7/32)*tCK 010 = Delay Y by (6/32)*tCK 011 = Delay Y by (5/32)*tCK 100 = Delay Y by (4/32)*tCK 101 = Delay Y by (3/32)*tCK 110 = Delay Y by (2/32)*tCK 111 = Delay Y by (1/32)*tCK | | |
| Note 1 Standard values for F1RC13 and F1RC12 are defined in the DDR3 LRDIMM Reference Design Specification for JEDEC standard module reference designs. | | | | | | | |

Byte 71 (Load Reduced): F1RC15 / F1RC14 - Additive Delay for QxODT and QxCKE

The control word location for the additive delay for QxODT signals for LRDIMMs is F1RC14. The control word location for the additive delay for the QxCKE control signals for LRDIMMs is F1RC15. This byte is referenced directly from the Memory Buffer specification.

| F1RC15 - Additive Delay for QxCKE, F1RC14 - Additive Delay for QxODT | | | | | | | |
|--|--|-----------|-----------|-----------------------------|--|-----------|-----------|
| F1RC15 | | | | F1RC14 | | | |
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| DBA1 value | DBA0 value | DA4 value | DA3 value | DBA1 value | DBA0 value | DA4 value | DA3 value |
| QxCKE Delay | | | | QxODT Delay | | | |
| 0 = Disabled 1 = Enabled | 000 = Delay QxCKE by (8/32)*tCK 001 = Delay QxCKE by (7/32)*tCK 010 = Delay QxCKE by (6/32)*tCK 011 = Delay QxCKE by (5/32)*tCK 100 = Delay QxCKE by (4/32)*tCK 101 = Delay QxCKE by (3/32)*tCK 110 = Delay QxCKE by (2/32)*tCK 111 = Delay QxCKE by (1/32)*tCK | | | 0 = Disabled 1 = Enabled | 000 = Delay QxODT by (8/32)*tCK 001 = Delay QxODT by (7/32)*tCK 010 = Delay QxODT by (6/32)*tCK 011 = Delay QxODT by (5/32)*tCK 100 = Delay QxODT by (4/32)*tCK 101 = Delay QxODT by (3/32)*tCK 110 = Delay QxODT by (2/32)*tCK 111 = Delay QxODT by (1/32)*tCK | | |
| Note 1 Standard values for F1RC15 and F1RC14 are defined in the DDR3 LRDIMM Reference Design Specification for JEDEC standard module reference designs. | | | | | | | |

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Byte 72 (Load Reduced): F3RC9 / F3RC8 - DRAM Interface MDQ Termination and Drive Strength for 800 & 1066

The control word location for the MDQ ODT strength for the LRDIMMs is F3RC8. The control word location for MDQ Driver Control for the LRDIMMs is F3RC9. This byte is referenced directly from the Memory Buffer specification. Applies to usage when the operating clock rate is $400 \leq f \leq 533$ MHz.

| F3RC9 - MDQ Driver Control, F3RC8 - MDQ Termination Strength for 800 & 1066 | | | | | | | |
|--|---|-----------|-----------|------------|---|-----------|-----------|
| F3RC9 | | | | F3RC8 | | | |
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| DBA1 value | DBA0 value | DA4 value | DA3 value | DBA1 value | DBA0 value | DA4 value | DA3 value |
| Reserved | MDQ Drive Strength | | | Reserved | MDQ ODT Strength | | |
| | 000 = RZQ/6 (40 Ω) 001 = RZQ/7 (34 Ω) 010 = RZQ/4 (48 Ω) 011 = RZQ/9 (27 Ω) 100 = RZQ/12 (20 Ω) 101 = Reserved 110 = Reserved 111 = Reserved | | | | 000 = DRAM Interface ODT disabled 001 = RZQ/4 (60 Ω) 010 = RZQ/2 (120 Ω) 011 = RZQ/6 (40 Ω) 100 = Reserved 101 = RZQ/8 (30 Ω) 110 = RZQ (240 Ω) 111 = RZQ/3 (80 Ω) | | |
| Note 1 Standard values for F3RC9 and F3RC8 are defined in the DDR3 LRDIMM Reference Design Specification for JEDEC standard module reference designs. | | | | | | | |

Byte 73 (Load Reduced): F[3,4]RC11 / F[3,4]RC10 - Rank 0&1 Read and Write QxODT Control for 800 & 1066

This byte defines the assertion for the QxODT[1:0] outputs for reads and writes from and to ranks 0 and 1. This byte is referenced directly from the Memory Buffer specification. Applies to usage when the operating clock rate is $400 \leq f \leq 533$ MHz

| F[3,4]RC11 - Write QxODT Control for Rank 0 & 1, F[3,4]RC10 - Read QxODT Control for Rank 0 & 1 for 800 & 1066 | | | | | | | |
|--|---|---|---|---|---|---|---|
| F4RC11 | | F3RC11 | | F4RC10 | | F3RC10 | |
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| DA4 value R1 | DA3 value R1 | DA4 value R0 | DA3 value R0 | DA4 value R1 | DA3 value R1 | DA4 value R0 | DA3 value R0 |
| QxODT1 0 = Not asserted during Write 1 = Asserted during Write | QxODT0 0 = Not asserted during Write 1 = Asserted during Write | QxODT1 0 = Not asserted during Write 1 = Asserted during Write | QxODT0 0 = Not asserted during Write 1 = Asserted during Write | QxODT1 0 = Not asserted during Read 1 = Asserted during Read | QxODT0 0 = Not asserted during Read 1 = Asserted during Read | QxODT1 0 = Not asserted during Read 1 = Asserted during Read | QxODT0 0 = Not asserted during Read 1 = Asserted during Read |
| Note 1 Standard values for F[3,4]RC11 and F[3,4]RC10 are defined in the DDR3 LRDIMM Reference Design Specification for JEDEC standard module reference designs. | | | | | | | |

Byte 74 (Load Reduced): F[5,6]RC11 / F[5,6]RC10 - Rank 2&3 Read and Write QxODT Control for 800 & 1066

This byte defines the assertion for the QxODT[1:0] outputs for reads and writes from and to ranks 2 and 3. This byte is referenced directly from the Memory Buffer specification. Applies to usage when the operating clock rate is $400 \leq f \leq 533$ MHz.

| F[5,6]RC11 - Write QxODT Control for Rank 2 & 3, F[5,6]RC10 - Read QxODT Control for Rank 2 & 3 for 800 & 1066 | | | | | | | |
|--|---|---|---|---|---|---|---|
| F6RC11 | | F5RC11 | | F6RC10 | | F5RC10 | |
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| DA4 value R3 | DA3 value R3 | DA4 value R2 | DA3 value R2 | DA4 value R3 | DA3 value R3 | DA4 value R2 | DA3 value R2 |
| QxODT1 0 = Not asserted during Write 1 = Asserted during Write | QxODT0 0 = Not asserted during Write 1 = Asserted during Write | QxODT1 0 = Not asserted during Write 1 = Asserted during Write | QxODT0 0 = Not asserted during Write 1 = Asserted during Write | QxODT1 0 = Not asserted during Read 1 = Asserted during Read | QxODT0 0 = Not asserted during Read 1 = Asserted during Read | QxODT1 0 = Not asserted during Read 1 = Asserted during Read | QxODT0 0 = Not asserted during Read 1 = Asserted during Read |
| Note 1 Standard values for F[3,4]RC11 and F[3,4]RC10 are defined in the DDR3 LRDIMM Reference Design Specification for JEDEC standard module reference designs. | | | | | | | |

Byte 75 (Load Reduced): F[7,8]RC11 / F[7,8]RC10 - Rank 4&5 Read and Write QxODT Control for 800 & 1066

This byte defines the assertion for the QxODT[1:0] outputs for reads and writes from and to ranks 4 and 5. This byte is referenced directly from the Memory Buffer specification. Applies to usage when the operating clock rate is $400 \leq f \leq 533$ MHz.

| F[7,8]RC11 - Write QxODT Control for Rank 4 & 5, F[7,8]RC10 - Read QxODT Control for Rank 4 & 5 for 800 & 1066 | | | | | | | |
|--|---|---|---|---|---|---|---|
| F8RC11 | | F7RC11 | | F8RC10 | | F7RC10 | |
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| DA4 value R5 | DA3 value R5 | DA4 value R4 | DA3 value R4 | DA4 value R5 | DA3 value R5 | DA4 value R4 | DA3 value R4 |
| QxODT1 0 = Not asserted during Write 1 = Asserted during Write | QxODT0 0 = Not asserted during Write 1 = Asserted during Write | QxODT1 0 = Not asserted during Write 1 = Asserted during Write | QxODT0 0 = Not asserted during Write 1 = Asserted during Write | QxODT1 0 = Not asserted during Read 1 = Asserted during Read | QxODT0 0 = Not asserted during Read 1 = Asserted during Read | QxODT1 0 = Not asserted during Read 1 = Asserted during Read | QxODT0 0 = Not asserted during Read 1 = Asserted during Read |
| Note 1 Standard values for F[3,4]RC11 and F[3,4]RC10 are defined in the DDR3 LRDIMM Reference Design Specification for JEDEC standard module reference designs. | | | | | | | |

Byte 76 (Load Reduced): F[9,10]RC11 / F[9,10]RC10 - Rank 6&7 Read and Write QxODT Control for 800 & 1066

This byte defines the assertion for the QxODT[1:0] outputs for reads and writes from and to ranks 6 and 7. This byte is referenced directly from the Memory Buffer specification. Applies to usage when the operating clock rate is $400 \leq f \leq 533$ MHz.

| F[9,10]RC11 - Write QxODT Control for Rank 6 & 7, F[9,10]RC10 - Read QxODT Control for Rank 6 & 7 for 800 & 1066 | | | | | | | |
|--|---|---|---|---|---|---|---|
| F10RC11 | | F9RC11 | | F10RC10 | | F9RC10 | |
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| DA4 value R7 | DA3 value R7 | DA4 value R6 | DA3 value R6 | DA4 value R7 | DA3 value R7 | DA4 value R6 | DA3 value R6 |
| QxODT1 0 = Not asserted during Write 1 = Asserted during Write | QxODT0 0 = Not asserted during Write 1 = Asserted during Write | QxODT1 0 = Not asserted during Write 1 = Asserted during Write | QxODT0 0 = Not asserted during Write 1 = Asserted during Write | QxODT1 0 = Not asserted during Read 1 = Asserted during Read | QxODT0 0 = Not asserted during Read 1 = Asserted during Read | QxODT1 0 = Not asserted during Read 1 = Asserted during Read | QxODT0 0 = Not asserted during Read 1 = Asserted during Read |
| Note 1 Standard values for F[3,4]RC11 and F[3,4]RC10 are defined in the DDR3 LRDIMM Reference Design Specification for JEDEC standard module reference designs. | | | | | | | |

Byte 77 (Load Reduced): MR1,2 for 800 & 1066

Bits[4:2] apply only to rank 0 and rank 1 (which are usually the termination ranks on the LRDIMM DRAM interface bus). The Memory Buffer SMBus addresses for the Rank 0 - 7 MR1,2 registers are 0xB8 - 0xBF. These bytes are referenced directly from the Memory Buffer specification. Applies to usage when the operating clock rate is $400 \leq f \leq 533$ MHz.

| MR1,2 Registers for 800 & 1066 | | | | | | | |
|--|-------|----------|--|-------|-------|--|-------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| DRAM Rtt_WR for all ranks | | Reserved | DRAM Rtt_Nom for ranks 0 and 1 | | | DRAM Driver Impedance for all ranks | |
| 00 = Dynamic ODT Off 01 = RZQ/4 (60 Ω) 10 = RZQ/2 (120 Ω) 11 = Reserved | | | 000 = Rtt_Nom disabled 001 = RZQ/4 (60 Ω) 010 = RZQ/2 (120 Ω) 011 = RZQ/6 (40 Ω) 100 = RZQ/12 (20 Ω) 101 = RZQ/8 (30 Ω) 110 = Reserved 111 = Reserved | | | 00 = RZQ/6 (40 Ω) 01 = RZQ/7 (34 Ω) 10 = RZQ/TBD 11 = RZQ/TBD | |
| Note 1 Rtt_Nom for ranks 2 to 7 must be programmed to '000' = Rtt_Nom disabled. Note 2 Standard values for this byte are defined in the DDR3 LRDIMM Reference Design Specification for JEDEC standard module reference designs. | | | | | | | |

Byte 78 (Load Reduced): F3RC9 / F3RC8 - DRAM Interface MDQ Termination and Drive Strength for 1333 & 1600

The control word location for the MDQ ODT strength for the LRDIMMs is F3RC8. The control word location for MDQ Driver Control for LRDIMMs is F3RC9. This byte is referenced directly from the Memory Buffer specification. Applies to usage when the operating clock rate is $533 < f \leq 800$ MHz.

| F3RC9 - MDQ Driver Control, F3RC8 - MDQ Termination Strength for 1333 & 1600 | | | | | | | |
|--|---|-----------|-----------|------------|---|-----------|-----------|
| F3RC9 | | | | F3RC8 | | | |
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| DBA1 value | DBA0 value | DA4 value | DA3 value | DBA1 value | DBA0 value | DA4 value | DA3 value |
| Reserved | MDQ Drive Strength | | | Reserved | MDQ ODT Strength | | |
| | 000 = RZQ/6 (40 Ω) 001 = RZQ/7 (34 Ω) 010 = RZQ/4 (48 Ω) 011 = RZQ/9 (27 Ω) 100 = RZQ/12 (20 Ω) 101 = Reserved 110 = Reserved 111 = Reserved | | | | 000 = DRAM Interface ODT disabled 001 = RZQ/4 (60 Ω) 010 = RZQ/2 (120 Ω) 011 = RZQ/6 (40 Ω) 100 = Reserved 101 = RZQ/8 (30 Ω) 110 = RZQ (240 Ω) 111 = RZQ/3 (80 Ω) | | |
| Note 1 Standard values for F3RC9 and F3RC8 are defined in the DDR3 LRDIMM Reference Design Specification for JEDEC standard module reference designs. | | | | | | | |

Byte 79 (Load Reduced): F[3,4]RC11 / F[3,4]RC10 - Rank 0&1 Read and Write QxODT Control for 1333 & 1600

This byte defines the assertion for the QxODT[1:0] outputs for reads and writes from and to rank 0. This byte is referenced directly from the Memory Buffer specification. Applies to usage when the operating clock rate is $533 < f \leq 800$ MHz.

| F[3,4]RC11 - Write QxODT Control for Rank 0 & 1, F[3,4]RC10 - Read QxODT Control for Rank 0 & 1 for 1333 & 1600 | | | | | | | |
|--|---|---|---|---|---|---|---|
| F4RC11 | | F3RC11 | | F4RC10 | | F3RC10 | |
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| DA4 value R1 | DA3 value R1 | DA4 value R0 | DA3 value R0 | DA4 value R1 | DA3 value R1 | DA4 value R0 | DA3 value R0 |
| QxODT1 0 = Not asserted during Write 1 = Asserted during Write | QxODT0 0 = Not asserted during Write 1 = Asserted during Write | QxODT1 0 = Not asserted during Write 1 = Asserted during Write | QxODT0 0 = Not asserted during Write 1 = Asserted during Write | QxODT1 0 = Not asserted during Read 1 = Asserted during Read | QxODT0 0 = Not asserted during Read 1 = Asserted during Read | QxODT1 0 = Not asserted during Read 1 = Asserted during Read | QxODT0 0 = Not asserted during Read 1 = Asserted during Read |
| Note 1 Standard values for F[3,4]RC11 and F[3,4]RC10 are defined in the DDR3 LRDIMM Reference Design Specification for JEDEC standard module reference designs. | | | | | | | |

Byte 80 (Load Reduced): F[5,6]RC11 / F[5,6]RC10 - Rank 2&3 Read and Write QxODT Control for 1333 & 1600

This byte defines the assertion for the QxODT[1:0] outputs for reads and writes from and to rank 0. This byte is referenced directly from the Memory Buffer specification. Applies to usage when the operating clock rate is $533 < f \leq 800$ MHz.

| F[5,6]RC11 - Write QxODT Control for Rank 2 & 3, F[5,6]RC10 - Read QxODT Control for Rank 2 & 3 for 1333 & 1600 | | | | | | | |
|--|---|---|---|---|---|---|---|
| F6RC11 | | F5RC11 | | F6RC10 | | F5RC10 | |
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| DA4 value R3 | DA3 value R3 | DA4 value R2 | DA3 value R2 | DA4 value R3 | DA3 value R3 | DA4 value R2 | DA3 value R2 |
| QxODT1 0 = Not asserted during Write 1 = Asserted during Write | QxODT0 0 = Not asserted during Write 1 = Asserted during Write | QxODT1 0 = Not asserted during Write 1 = Asserted during Write | QxODT0 0 = Not asserted during Write 1 = Asserted during Write | QxODT1 0 = Not asserted during Read 1 = Asserted during Read | QxODT0 0 = Not asserted during Read 1 = Asserted during Read | QxODT1 0 = Not asserted during Read 1 = Asserted during Read | QxODT0 0 = Not asserted during Read 1 = Asserted during Read |
| Note 1 Standard values for F[3,4]RC11 and F[3,4]RC10 are defined in the DDR3 LRDIMM Reference Design Specification for JEDEC standard module reference designs. | | | | | | | |

Byte 81 (Load Reduced): F[7,8]RC11 / F[7,8]RC10 - Rank 4&5 Read and Write QxODT Control for 1333 & 1600

This byte defines the assertion for the QxODT[1:0] outputs for reads and writes from and to rank 0. This byte is referenced directly from the Memory Buffer specification. Applies to usage when the operating clock rate is $533 < f \leq 800$ MHz.

| F[7,8]RC11 - Write QxODT Control for Rank 4 & 5, F[7,8]RC10 - Read QxODT Control for Rank 4 & 5 for 1333 & 1600 | | | | | | | |
|--|---|---|---|---|---|---|---|
| F8RC11 | | F7RC11 | | F8RC10 | | F7RC10 | |
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| DA4 value R5 | DA3 value R5 | DA4 value R4 | DA3 value R4 | DA4 value R5 | DA3 value R5 | DA4 value R4 | DA3 value R4 |
| QxODT1 0 = Not asserted during Write 1 = Asserted during Write | QxODT0 0 = Not asserted during Write 1 = Asserted during Write | QxODT1 0 = Not asserted during Write 1 = Asserted during Write | QxODT0 0 = Not asserted during Write 1 = Asserted during Write | QxODT1 0 = Not asserted during Read 1 = Asserted during Read | QxODT0 0 = Not asserted during Read 1 = Asserted during Read | QxODT1 0 = Not asserted during Read 1 = Asserted during Read | QxODT0 0 = Not asserted during Read 1 = Asserted during Read |
| Note 1 Standard values for F[3,4]RC11 and F[3,4]RC10 are defined in the DDR3 LRDIMM Reference Design Specification for JEDEC standard module reference designs. | | | | | | | |

Byte 82 (Load Reduced): F[9,10]RC11 / F[9,10]RC10 - Rank 6&7 Read and Write QxODT Control for 1333 & 1600

This byte defines the assertion for the QxODT[1:0] outputs for reads and writes from and to rank 0. This byte is referenced directly from the Memory Buffer specification. Applies to usage when the operating clock rate is $533 < f \leq 800$ MHz.

| F[9,10]RC11 - Write QxODT Control for Rank 6 & 7, F[9,10]RC10 - Read QxODT Control for Rank 6 & 7 for 1333 & 1600 | | | | | | | |
|--|---|---|---|---|---|---|---|
| F10RC11 | | F9RC11 | | F10RC10 | | F9RC10 | |
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| DA4 value R7 | DA3 value R7 | DA4 value R6 | DA3 value R6 | DA4 value R7 | DA3 value R7 | DA4 value R6 | DA3 value R6 |
| QxODT1 0 = Not asserted during Write 1 = Asserted during Write | QxODT0 0 = Not asserted during Write 1 = Asserted during Write | QxODT1 0 = Not asserted during Write 1 = Asserted during Write | QxODT0 0 = Not asserted during Write 1 = Asserted during Write | QxODT1 0 = Not asserted during Read 1 = Asserted during Read | QxODT0 0 = Not asserted during Read 1 = Asserted during Read | QxODT1 0 = Not asserted during Read 1 = Asserted during Read | QxODT0 0 = Not asserted during Read 1 = Asserted during Read |
| Note 1 Standard values for F[3,4]RC11 and F[3,4]RC10 are defined in the DDR3 LRDIMM Reference Design Specification for JEDEC standard module reference designs. | | | | | | | |

Byte 83 (Load Reduced): MR1,2 for 1333 & 1600

Bits[4:2] apply only to rank 0 and rank 1 (which are usually the termination ranks on the LRDIMM DRAM interface bus). The Memory Buffer SMBus addresses for the Rank 0 - 7 MR1,2 registers are 0xB8 - 0xBF. These bytes are referenced directly from the Memory Buffer specification. Applies to usage when the operating clock rate is $533 < f \leq 800$ MHz.

| MR1,2 Registers for 1333 & 1600 | | | | | | | |
|--|-------|----------|--|-------|-------|--|-------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| DRAM Rtt_WR for all ranks | | Reserved | DRAM Rtt_Nom for ranks 0 and 1 | | | DRAM Driver Impedance for all ranks | |
| 00 = Dynamic ODT Off 01 = RZQ/4 (60 Ω) 10 = RZQ/2 (120 Ω) 11 = Reserved | | | 000 = Rtt_Nom disabled 001 = RZQ/4 (60 Ω) 010 = RZQ/2 (120 Ω) 011 = RZQ/6 (40 Ω) 100 = RZQ/12 (20 Ω) 101 = RZQ/8 (30 Ω) 110 = Reserved 111 = Reserved | | | 00 = RZQ/6 (40 Ω) 01 = RZQ/7 (34 Ω) 10 = RZQ/TBD 11 = RZQ/TBD | |
| Note 1 Rtt_Nom for ranks 2 to 7 must be programmed to '000' = Rtt_Nom disabled. Note 2 Standard values for this byte are defined in the DDR3 LRDIMM Reference Design Specification for JEDEC standard module reference designs. | | | | | | | |

Byte 84 (Load Reduced): F3RC9 / F3RC8 - DRAM Interface MDQ Termination and Drive Strength for 1866 & 2133

The control word location for the MDQ ODT strength for LRDIMMs is F3RC8. The control word location for MDQ Driver Control for LRDIMMs is F3RC9. This byte is referenced directly from the Memory Buffer specification. Applies to usage when the operating clock rate is $800 < f \leq 1067$ MHz.

| F3RC9 - MDQ Driver Control, F3RC8 - MDQ Termination Strength for 1866 & 2133 | | | | | | | |
|--|---|-----------|-----------|------------|---|-----------|-----------|
| F3RC9 | | | | F3RC8 | | | |
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| DBA1 value | DBA0 value | DA4 value | DA3 value | DBA1 value | DBA0 value | DA4 value | DA3 value |
| Reserved | MDQ Drive Strength | | | Reserved | MDQ ODT Strength | | |
| | 000 = RZQ/6 (40 Ω) 001 = RZQ/7 (34 Ω) 010 = RZQ/4 (48 Ω) 011 = RZQ/9 (27 Ω) 100 = RZQ/12 (20 Ω) 101 = Reserved 110 = Reserved 111 = Reserved | | | | 000 = DRAM Interface ODT disabled 001 = RZQ/4 (60 Ω) 010 = RZQ/2 (120 Ω) 011 = RZQ/6 (40 Ω) 100 = Reserved 101 = RZQ/8 (30 Ω) 110 = RZQ (240 Ω) 111 = RZQ/3 (80 Ω) | | |
| Note 1 Standard values for F3RC9 and F3RC8 are defined in the DDR3 LRDIMM Reference Design Specification for JEDEC standard module reference designs. | | | | | | | |

Byte 85 (Load Reduced): F[3,4]RC11 / F[3,4]RC10 - Rank 0&1 Read and Write QxODT Control for 1866 & 2133

This byte defines the assertion for the QxODT[1:0] outputs for reads and writes from and to rank 0. This byte is referenced directly from the Memory Buffer specification. Applies to usage when the operating clock rate is $800 < f \leq 1067$ MHz.

| F[3,4]RC11 - Write QxODT Control for Rank 0 & 1, F[3,4]RC10 - Read QxODT Control for Rank 0 & 1 for 1866 & 2133 | | | | | | | |
|--|---|---|---|---|---|---|---|
| F4RC11 | | F3RC11 | | F4RC10 | | F3RC10 | |
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| DA4 value R1 | DA3 value R1 | DA4 value R0 | DA3 value R0 | DA4 value R1 | DA3 value R1 | DA4 value R0 | DA3 value R0 |
| QxODT1 0 = Not asserted during Write 1 = Asserted during Write | QxODT0 0 = Not asserted during Write 1 = Asserted during Write | QxODT1 0 = Not asserted during Write 1 = Asserted during Write | QxODT0 0 = Not asserted during Write 1 = Asserted during Write | QxODT1 0 = Not asserted during Read 1 = Asserted during Read | QxODT0 0 = Not asserted during Read 1 = Asserted during Read | QxODT1 0 = Not asserted during Read 1 = Asserted during Read | QxODT0 0 = Not asserted during Read 1 = Asserted during Read |
| Note 1 Standard values for F[3,4]RC11 and F[3,4]RC10 are defined in the DDR3 LRDIMM Reference Design Specification for JEDEC standard module reference designs. | | | | | | | |

Byte 86 (Load Reduced): F[5,6]RC11 / F[5,6]RC10 - Rank 2&3 Read and Write QxODT Control for 1866 & 2133

This byte defines the assertion for the QxODT[1:0] outputs for reads and writes from and to rank 0. This byte is referenced directly from the Memory Buffer specification. Applies to usage when the operating clock rate is $800 < f \leq 1067$ MHz.

| F[5,6]RC11 - Write QxODT Control for Rank 2 & 3, F[5,6]RC10 - Read QxODT Control for Rank 2 & 3 for 1866 & 2133 | | | | | | | |
|--|---|---|---|---|---|---|---|
| F6RC11 | | F5RC11 | | F6RC10 | | F5RC10 | |
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| DA4 value R3 | DA3 value R3 | DA4 value R2 | DA3 value R2 | DA4 value R3 | DA3 value R3 | DA4 value R2 | DA3 value R2 |
| QxODT1 0 = Not asserted during Write 1 = Asserted during Write | QxODT0 0 = Not asserted during Write 1 = Asserted during Write | QxODT1 0 = Not asserted during Write 1 = Asserted during Write | QxODT0 0 = Not asserted during Write 1 = Asserted during Write | QxODT1 0 = Not asserted during Read 1 = Asserted during Read | QxODT0 0 = Not asserted during Read 1 = Asserted during Read | QxODT1 0 = Not asserted during Read 1 = Asserted during Read | QxODT0 0 = Not asserted during Read 1 = Asserted during Read |
| Note 1 Standard values for F[3,4]RC11 and F[3,4]RC10 are defined in the DDR3 LRDIMM Reference Design Specification for JEDEC standard module reference designs. | | | | | | | |

Byte 87 (Load Reduced): F[7,8]RC11 / F[7,8]RC10 - Rank 4&5 Read and Write QxODT Control for 1866 & 2133

This byte defines the assertion for the QxODT[1:0] outputs for reads and writes from and to rank 0. This byte is referenced directly from the Memory Buffer specification. Applies to usage when the operating clock rate is $800 < f \leq 1067$ MHz.

| F[7,8]RC11 - Write QxODT Control for Rank 4 & 5, F[7,8]RC10 - Read QxODT Control for Rank 4 & 5 for 1866 & 2133 | | | | | | | |
|--|---|---|---|---|---|---|---|
| F8RC11 | | F7RC11 | | F8RC10 | | F7RC10 | |
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| DA4 value R5 | DA3 value R5 | DA4 value R4 | DA3 value R4 | DA4 value R5 | DA3 value R5 | DA4 value R4 | DA3 value R4 |
| QxODT1 0 = Not asserted during Write 1 = Asserted during Write | QxODT0 0 = Not asserted during Write 1 = Asserted during Write | QxODT1 0 = Not asserted during Write 1 = Asserted during Write | QxODT0 0 = Not asserted during Write 1 = Asserted during Write | QxODT1 0 = Not asserted during Read 1 = Asserted during Read | QxODT0 0 = Not asserted during Read 1 = Asserted during Read | QxODT1 0 = Not asserted during Read 1 = Asserted during Read | QxODT0 0 = Not asserted during Read 1 = Asserted during Read |
| Note 1 Standard values for F[3,4]RC11 and F[3,4]RC10 are defined in the DDR3 LRDIMM Reference Design Specification for JEDEC standard module reference designs. | | | | | | | |

Byte 88 (Load Reduced): F[9,10]RC11 / F[9,10]RC10 - Rank 6&7 Read and Write QxODT Control for 1866 & 2133

This byte defines the assertion for the QxODT[1:0] outputs for reads and writes from and to rank 0. This byte is referenced directly from the Memory Buffer specification. Applies to usage when the operating clock rate is $800 < f \leq 1067$ MHz.

| F[9,10]RC11 - Write QxODT Control for Rank 6 & 7, F[9,10]RC10 - Read QxODT Control for Rank 6 & 7 for 1866 & 2133 | | | | | | | |
|--|---|---|---|---|---|---|---|
| F10RC11 | | F9RC11 | | F10RC10 | | F9RC10 | |
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| DA4 value R7 | DA3 value R7 | DA4 value R6 | DA3 value R6 | DA4 value R7 | DA3 value R7 | DA4 value R6 | DA3 value R6 |
| QxODT1 0 = Not asserted during Write 1 = Asserted during Write | QxODT0 0 = Not asserted during Write 1 = Asserted during Write | QxODT1 0 = Not asserted during Write 1 = Asserted during Write | QxODT0 0 = Not asserted during Write 1 = Asserted during Write | QxODT1 0 = Not asserted during Read 1 = Asserted during Read | QxODT0 0 = Not asserted during Read 1 = Asserted during Read | QxODT1 0 = Not asserted during Read 1 = Asserted during Read | QxODT0 0 = Not asserted during Read 1 = Asserted during Read |
| Note 1 Standard values for F[3,4]RC11 and F[3,4]RC10 are defined in the DDR3 LRDIMM Reference Design Specification for JEDEC standard module reference designs. | | | | | | | |

Byte 89 (Load Reduced): MR1,2 for 1866 & 2133

Bits[4:2] apply only to rank 0 and rank 1 (which are usually the termination ranks on the LRDIMM DRAM interface bus). The Memory Buffer SMBus addresses for the Rank 0 - 7 MR1,2 registers are 0xB8 - 0xBF. These bytes are referenced directly from the Memory Buffer specification. Applies to usage when the operating clock rate is $800 < f \leq 1067$ MHz.

| MR1,2 Registers for 1866 & 2133 | | | | | | | |
|---|-------|----------|--|-------|-------|--|-------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| DRAM Rtt_WR for all ranks | | Reserved | DRAM Rtt_Nom for ranks 0 and 1 | | | DRAM Driver Impedance for all ranks | |
| 00 = Dynamic ODT Off 01 = RZQ/4 (60 Ω) 10 = RZQ/2 (120 Ω) 11 = Reserved | | | 000 = Rtt_Nom disabled 001 = RZQ/4 (60 Ω) 010 = RZQ/2 (120 Ω) 011 = RZQ/6 (40 Ω) 100 = RZQ/12 (20 Ω) 101 = RZQ/8 (30 Ω) 110 = Reserved 111 = Reserved | | | 00 = RZQ/6 (40 Ω) 01 = RZQ/7 (34 Ω) 10 = RZQ/TBD 11 = RZQ/TBD | |
| <p>Note 1 Rtt_Nom for ranks 2 to 7 must be programmed to '000' = Rtt_Nom disabled.</p> <p>Note 2 Standard values for this byte are defined in the DDR3 LRDIMM Reference Design Specification for JEDEC standard module reference designs.</p> | | | | | | | |

Byte 90 (Load Reduced): Minimum Module Delay Time for 1.5 V

This byte defines the minimum delay for the earliest byte lane of the module for 1.5 V, in medium timebase (MTB) units.

| Bit 7 | Bits 6 ~ 0 |
|--|---|
| Reserved | Minimum Delay Time for 1.5 V |
| | Values defined from: 0000000 = 0 (0 ns) to 1111111 = 127 (15.875 ns) |
| <p>Note 1 This delay is defined for the specific prelaunch delay settings from LRDIMM SPD bytes 69 to 71.</p> <p>Note 2 This delay does not include delays created by utilizing "Additional DQ/DQS Read Delay Control Words F[3-11]RC12.</p> | |

Byte 91 (Load Reduced): Maximum Module Delay for 1.5 V

This byte defines the maximum delay for the latest byte lane of the module for 1.5 V, in medium timebase (MTB) units.

| Bit 7 | Bits 6 ~ 0 |
|--|---|
| Reserved | Maximum Delay Time for 1.5 V |
| | Values defined from: 0000000 = 0 (0 ns) to 1111111 = 127 (15.875 ns) |
| <p>Notes: This delay is defined for the specific prelaunch delay settings from LRDIMM SPD bytes 69 to 71. This delay does not include delays created by utilizing "Additional DQ/DQS Read Delay Control Words F[3-11]RC12.</p> | |

Byte 92 (Load Reduced): Minimum Module Delay for 1.35 V

This byte defines the minimum delay for the earliest byte lane of the module for 1.35 V, in medium timebase (MTB) units.

| Bit 7 | Bits 6 ~ 0 |
|--|---|
| Reserved | Minimum Delay Time for 1.35 V |
| | Values defined from: 0000000 = 0 (0 ns) to 1111111 = 127 (15.875 ns) |
| Note 1 This delay is defined for the specific prelaunch delay settings from LRDIMM SPD bytes 69 to 71. | |
| Note 2 This delay does not include delays created by utilizing "Additional DQ/DQS Read Delay Control Words F[3-11]RC12. | |

Byte 93 (Load Reduced): Maximum Module Delay Time for 1.35 V

This byte defines the maximum delay for the latest byte lane of the module for 1.35 V, in medium timebase (MTB) units.

| Bit 7 | Bits 6 ~ 0 |
|---|---|
| Reserved | Maximum Delay Time for 1.35 V |
| | Values defined from: 0000000 = 0 (0 ns) to 1111111 = 127 (15.875 ns) |
| Notes: This delay is defined for the specific prelaunch delay settings from LRDIMM SPD bytes 69 to 71. This delay does not include delays created by utilizing "Additional DQ/DQS Read Delay Control Words F[3-11]RC12. | |

Byte 94 (Load Reduced): Minimum Module Delay Time for 1.25 V

This byte defines the minimum delay for the earliest byte lane of the module for 1.25 V, in medium timebase (MTB) units.

| Bit 7 | Bits 6 ~ 0 |
|--|---|
| Reserved | Minimum Delay Time for 1.25 V |
| | Values defined from: 0000000 = 0 (0 ns) to 1111111 = 127 (15.875 ns) |
| Note 1 This delay is defined for the specific prelaunch delay settings from LRDIMM SPD bytes 69 to 71. | |
| Note 2 This delay does not include delays created by utilizing "Additional DQ/DQS Read Delay Control Words F[3-11]RC12. | |

Byte 95 (Load Reduced): Maximum Module Delay Time for 1.25 V

This byte defines the maximum delay for the latest byte lane of the module for 1.25 V, in medium timebase (MTB) units.

| Bit 7 | Bits 6 ~ 0 |
|---|---|
| Reserved | Maximum Delay Time for 1.25 V |
| | Values defined from: 0000000 = 0 (0 ns) to 1111111 = 127 (15.875 ns) |
| Note 1 This delay is defined for the specific prelaunch delay settings from LRDIMM SPD bytes 69 to 71. Note 2 This delay does not include delays created by utilizing "Additional DQ/DQS Read Delay Control Words F[3-11]RC12. | |

Bytes 96 ~ 101 (Load Reduced): Reserved

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Bytes 102 ~ 116 (Load Reduced): Memory Buffer Personality Bytes

The Personality Bytes for the Load Reduced DIMM Memory Buffer are listed, and the specific .

| Memory Buffer Personality Bytes for Load Reduced Module Types | | | |
|---|---------------------|--------------------------|----------|
| Byte Number | Function Described | Destination ¹ | |
| | | Bits 7~4 | Bits 3~0 |
| 102 | Personality Byte 0 | F14RC1 | F14RC0 |
| 103 | Personality Byte 1 | F14RC3 | F14RC2 |
| 104 | Personality Byte 2 | F14RC5 | F14RC4 |
| 105 | Personality Byte 3 | F15RC6 | F14RC6 |
| 106 | Personality Byte 4 | F14RC9 | F14RC8 |
| 107 | Personality Byte 5 | F14RC11 | F14RC10 |
| 108 | Personality Byte 6 | F14RC13 | F14RC12 |
| 109 | Personality Byte 7 | F14RC15 | F14RC14 |
| 110 | Personality Byte 8 | F15RC1 | F15RC0 |
| 111 | Personality Byte 9 | F15RC3 | F15RC2 |
| 112 | Personality Byte 10 | F15RC5 | F15RC4 |
| 113 | Personality Byte 11 | F15RC9 | F15RC8 |
| 114 | Personality Byte 12 | F15RC11 | F15RC10 |
| 115 | Personality Byte 13 | F15RC13 | F15RC12 |
| 116 | Personality Byte 14 | F15RC15 | F15RC14 |

Note 1 The manufacturer specific personality bytes are copied into these Memory Buffer control words.

Manufacturer's Specific Bytes for Load Reduced Memory Module Types (Bytes 150 ~ 175): Reserved for manufacturer or user

Note that in early revisions of the LRDIMM SPD, this section contained personality byte data which has been relocated to the DIMM-specific region of the SPD. From LRDIMM SPD revision 0.5 on, this section is open for manufacturer specific information.